



CFA Institute[®]

CFA Institute Research Challenge

Hosted by
CFA Society Italy

Pepper Hill

The CFA Institute Research Challenge is a global competition that tests the equity research and valuation, investment report writing, and presentation skills of university students. The following report was prepared in compliance with the Official Rules of the CFA Institute Research Challenge, is submitted by a team of university students as part of this annual educational initiative and should not be considered a professional report.

Disclosures:

Ownership and material conflicts of interest:

The author(s), or a member of their household, of this report does not hold a financial interest in the securities of this company. The author(s), or a member of their household, of this report does not know of the existence of any conflicts of interest that might bias the content or publication of this report.

Receipt of compensation:

Compensation of the author(s) of this report is not based on investment banking revenue.

Position as a officer or director:

The author(s), or a member of their household, does not serve as an officer, director or advisory board member of the subject company.

Market making:

The author(s) does not act as a market maker in the subject company's securities.

Disclaimer:

The information set forth herein has been obtained or derived from sources generally available to the public and believed by the author(s) to be reliable, but the author(s) does not make any representation or warranty, express or implied, as to its accuracy or completeness. The information is not intended to be used as the basis of any investment decisions by any person or entity. This information does not constitute investment advice, nor is it an offer or a solicitation of an offer to buy or sell any security. This report should not be considered to be a recommendation by any individual affiliated with CFA Society Italy, CFA Institute or the CFA Institute Research Challenge with regard to this company's stock.

Initiation of coverage | 1st February 2026

Italy | Technology | Semiconductor Testing Equipment

HOLD

Current Price	€15.63
Target Price	€15.38
Downside	1.6%
Total Shareholder Return	-1.6%

Listed on: Euronext Milan
 Ticker: TPRO-IT

Market Data

Main Shareholders

T-Plus S.p.A.	56.43%
Teradyne, Inc.	10.00%
Corporacion Financiera Alba	6.01%
Wertheimer Ruth	3.70%
Treasury Shares	1.98%
Free Float	23%

Shares Outstanding [m] **653.26**

Market Cap [€bn] **10.21**

Stock Data

52 w H/L [€]	16.60/4.77
Avg. Daily Volume (52w) [m]	0.164

Key Financials

	FY25E	FY26E	FY27E
EPS	0.14	0.27	0.37
DPS	/	/	/
Dividend Yield	/	/	/
Price to Book	8.24x	7.23x	6.17x
ROE	8.3%	12.6%	15.4%
ROIC	17%	27.5%	33.2%

4Y Price Performance



Source: Team Elaboration

Technoprobe S.p.A.

Investment Summary

We initiate our coverage on Technoprobe S.p.A. (TPRO) with a **HOLD recommendation** and a year-end target price of €15.38, implying a 1.6% downside from the closing price of €15.63 on January 30, 2026.

With a Market Cap of **€10bn** and €626m sales in FY25E, TPRO is a leading company in the semiconductor testing industry. Leveraging its global manufacturing expertise and its strategic positioning along the semiconductor supply chain, the Company has consistently delivered solid financial performance, with **best-in-class EBIT margin** (24% in FY25E) and strong **Cash Flow generation** (16% FCF/Revenues in FY25E). Since its IPO on Euronext Milan in 2023, TPRO's share price has traded largely sideways until November 2025, when it **rocketed to a peak** of €13.75. The move was supported by sharp EV/EBITDA re-rating (from 33.78x to 51.46x), following bullish outlook on capacity expansion and progress in High Bandwidth Memory (HBM) customer qualification, a structurally growing AI-driven segment. Momentum strengthened further in January 2026 after TSMC's Q4 results, which pointed to accelerating AI-driven demand and reinforced expectations of sustained semiconductor CapEx, confirming the **stock's strong correlation** with AI leaders (*Exhibit 1*).

At current valuation levels, we do believe the share price **already reflects** the Company's strong growth outlook (23.4% CAGR FY25E-30E) after an impressive rally (+111% 6M performance). Moreover, we remain cautious regarding: (i) persistent **operational constraints**, as high capacity utilization leaves limited headroom for expansion; (ii) **intensifying competition** within the Logic segment; and (iii) **uncertainty** surrounding the timing of the HBM technological roadmap.

	2023	2024	2025E	2026E	2027E	2028E	2029E	2030E
Revenues [€m]	409	543	626	754	947	1,172	1,466	1,792
EBITDA [€m]	122	136	217	301	397	445	586	753
Margin	30%	25%	35%	40%	42%	38%	40%	42%
Net Income [€m]	97	62	111	173	242	269	374	497
Margin	24%	12%	18%	23%	26%	23%	26%	28%
FCFF [€m]	43	21	106	100	118	197	281	340
EPS [€]	0.16	0.10	0.14	0.27	0.37	0.41	0.57	0.76
EV/EBITDA	39.3x	22.4x	33.5x	31.6x	24.0x	21.4x	16.2x	12.6x
EV/CE	7.8x	8.3x	12.2x	14.2x	12.0x	11.0x	9.9x	8.5x
P/E	53.5x	56.8x	87.1x	58.8x	42.1x	37.9x	27.3x	20.5x
Net Debt [€m]	(348)	(655)	(704)	(742)	(779)	(881)	(103)	(121)

On the Testing Throne: TPRO's Mastery of MEMS

TPRO is an **Italy-based** company founded in 1996 by the Crippa family (69.3% of voting rights). The Company specialises in the design and manufacture of **probe cards** (80.3% FY25E Revenues), a key component used for the electrical test on wafer for chips (CPUs, GPUs). Moreover, after DIS Tech acquisition in 2024, TPRO entered final testing, the last stage of the semiconductor testing process (19.7% FY25E Revenues). TPRO's proprietary **Vertical MEMS** technology (TPEG™), protected by a portfolio of more than **600 patents**, is widely regarded as best-in-class for high-end Logic devices. On this technological foundation, the Group has built a global leadership position, with a **60% market share** in the Logic Vertical MEMS probe cards, serving global leading players of advance chips (*Exhibit 4*).

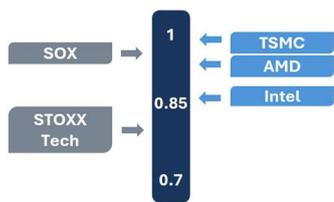
This positioning translates into a distinctive financial profile (20% FY19-25E Revenues CAGR), **best-in-class profitability** (35% FY25E EBITDA margin) and a strong net cash position (FY25E €704m, 7% of Market Cap), providing strategic flexibility to sustain R&D, CapEx and potential technology-driven M&A. Despite a contraction registered in FY23-24, the Company is expected to reach approximately €626m revenues in FY25E (+15% YoY), primarily supported by the first full-year consolidation of DIS Tech (€125m FY25E revenues) and the growth in the AI segment (36% of TPRO revenues).

In addition, the relevance of Vertical MEMS technology is expected to further increase with exposure to **high-growth segments**, such as High Bandwidth Memory (HBM) and Silicon Photonics (SiPh), where AI-related demand is driving more stringent testing requirements. However, we do see high uncertainty around the timing of adoption and we do believe these opportunities are unlikely to become material before FY27-28.

...but the Frontier is Crowding: Capacity Constraints and Rivalry in New Lands

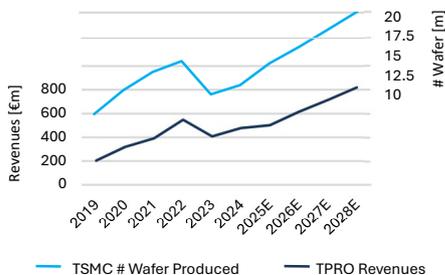
While the AI driven boom in the logic segment provides a powerful tailwind, TPRO's growth trajectory is subject to several structural constraints that, in our view, limit near term upside: (i) **production capacity** is already operating at **90% utilization rate**, making it difficult to outpace the 22% expected CAGR FY25E-27E. As a result, TPRO may not fully capture rising demand for probe cards needed to test the higher volumes of AI chips, driven by a 50% increase in Hyperscaler CapEx in FY26E; (ii) the logic probe card market itself **presents inherent limitations**; increase in market share seems to be unlikely due to clients' multiple sources policy and **rising competitive pressure** from FormFactor (main competitor) and Taiwanese players closely connected to TSMC (main TPRO's client and main logic chip manufacturer). This marks a sharp contrast with the 2019-2022 period, when TPRO outpaced the market (39% CAGR vs. 22% market CAGR), performance that appears difficult to replicate in the future; (iii) challenges are even greater in new markets; SiPh and HBM testing are both characterised by **high uncertainty**. More specifically, the HBM adoption depends heavily on customer timing and strategic choices, while strong incumbents with long-standing relationships, such as FormFactor and SK Hynix (Memory chip manufacturer), create **high barriers to entry**. As a result, a delayed/failure in gaining 20% market share (our base case) could result in 9.67% downside on FY28E EBITDA.

Price correlation – Exhibit 1



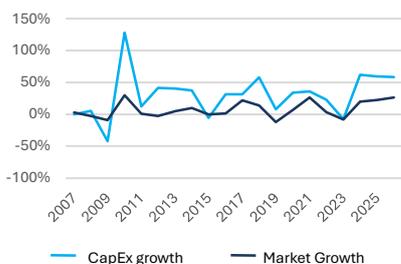
Source: Company Data, Team Estimates

Technoprobe Revenues and TSMC Wafer Production Correlation – Exhibit 2



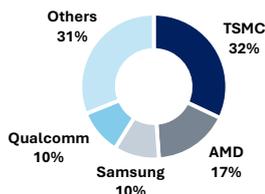
Source: Company Data, Team Estimates

Semiconductor Market vs Hyperscaler CapEx cycle – Exhibit 3



Source: Company Data, Team Estimates

FY25 Revenue Contribution by Customer – Exhibit 4



Source: Company Data, Team Estimates

A Heavy Crown: When Engineering Supremacy meets Capital Inefficiency

M&A strategy and capital allocation: TPRO’s technological positioning is driven by a management team with strong engineering expertise, able to anticipate long-term trends in advanced semiconductor testing. However, the translation of this strategic vision into sustainable economic and financial value has been materially less effective. Past M&A transactions and vertical integration initiatives, while broadly coherent from an industrial standpoint, have failed to generate commensurate financial returns: sharp decrease in profitability (EBITDAm from 30% FY23 to 25% FY24), a progressive deterioration in returns on capital (ROIC-ex goodwill from 16% FY23 to 8% FY24) and the closure of underperforming assets, Harbor Electronics and Microfabrica plants. The shutdown of Harbor, due to its inability to achieve industrial scale and acceptable returns, created a structural gap in TPRO’s final test offering. The original plan to fully internalise the Final Testing value chain failed, leaving only the design component in place through DIS Tech (acquired from Teradyne).

While the DIS Tech transaction provides an immediate revenue contribution (€125m expected in FY25E), it came at the cost of 10% equity dilution and the inclusion of Teradyne’s CEO on TPRO’s Board, increasing Teradyne’s influence without a clear strategic payoff as it is struggling to keep up with the AI application.

Financial management and investor appeal: In parallel, TPRO adopts a bread & butter approach to financial risk management, most notably the absence of FX hedging despite approximately 90% of earnings being USD-denominated, leaving revenues and margins structurally exposed to USD/EUR volatility (the 1400bps depreciation of USD resulted in -11% FX/Sales in FY25). Additionally, we consider as a further cautionary factor the presence of a structurally low free float (23% of €10bn market cap) which reduces the stock’s appeal to a broader institutional investor base, limiting liquidity and potentially amplifying share price volatility.

Investment risk

Operating in the semiconductor industry entails elevated structural risk, driven by pronounced cyclicality: in the last 20 years analysed, the industry has experienced on average a material contraction of 7% every five years (Exhibit 3). AI-driven demand further amplifies this risk, exposing the Company to volatile Hyperscaler CapEx cycles (\$600B expected in 2026) and the heightened risk of capacity oversupply if growth expectations fail to materialize. Additionally, in the short to medium term, TPRO’s idiosyncratic risks are primarily business and market-specific, notably (i) the execution risks associated with doubling production capacity, (ii) a delayed entry into the HBM segment, which could adversely affect market share if the adoption of Vertical MEMS technology lags behind expectations and (iii) a persistent structural pressures from an unmanaged FX exposure.

Over the longer term, risks are mainly competitive, including (i) intensifying pressure from state-backed Chinese companies and other price-aggressive Asian players, and (ii) a rapid technological evolution in which rivals’ intensifying R&D and potential IP leakage could compromise TPRO’s strategic positioning.

Valuation

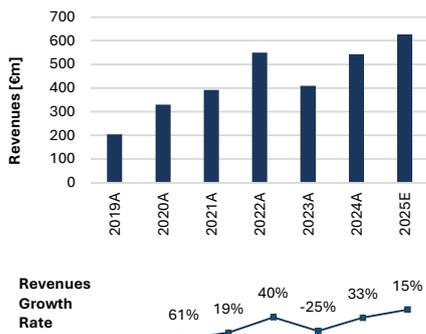
Our year-end target price of €15.38 is derived from a valuation using a three-stages asset-side DCF. The model applies a WACC of 9.21% and a 4% terminal growth rate, capturing both the cash flows generated by TPRO’s Logic business and the longer-term growth potential from its entry into the HBM and Silicon Photonics segment. The DCF is structured around three distinct phases reflecting the evolution of TPRO’s business profile across the cycle. In the first stage, we expect an AI-driven expansion, with revenues growing at a 19.15% CAGR over FY25E-30E, supported by the Company’s entry into HBM and SiPh segment, additionally to its core Logic business. In the second stage, we assume a transition toward a more mature growth profile, with TPRO expected to achieve a moderate penetration in the memory and photonics segment (respectively 35% and 30% market share). Revenue growth is projected to normalize to a 9.7% CAGR over FY30-35, gradually converging toward the structural terminal growth of 4%, implying a terminal value of €6,886m (73.69% of EV).

A relative valuation provides further support for the DCF outcome. TPRO’s valuation is assessed using a forward-looking multiples framework, benchmarked against a peer group with comparable business models, capital intensity and exposure to attractive long-term semiconductor trends. Using a 1-year forward EV/CE multiple regressed against 1-year forward ROCE, TPRO currently trades at a 9.86% discount to peers, implying a target equity value of €15.83 per share. This result is closely aligned with our DCF estimate (€15.38 per share) and the current share price, reinforcing the consistency of our valuation and supporting a HOLD recommendation.



Business Description

TPRO's revenue growth – Exhibit 5



Source: Team Elaboration

Value-chain funnel & TPRO sweet spot – Exhibit 6



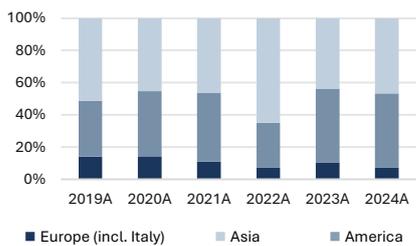
Source: Team Elaboration

TPRO operating segments, product categories and types – Exhibit 7

Group	Technoprobe S.p.A.				
Op. Segments	Wafer-level test			Final Test	
Product Category	Probe Cards			Device Interface Solutions	
Product Type	Vertical MEMS	Vertical	Cantilever	DIB	Test Socket

Source: Team Elaboration

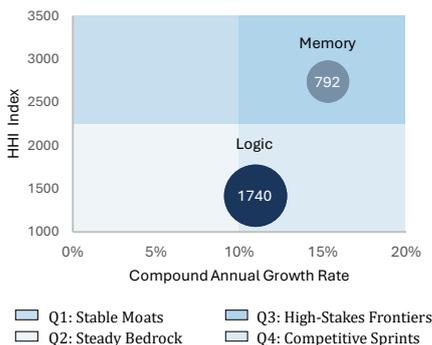
Revenues breakdown by geography – Exhibit 8



Source: Company Data, Team Estimates

Logic vs. Memory Market – Exhibit 9

Bubble size: 2024 Market Size (\$b)



Source: Market Data, Team Elaboration

With a Market Cap of approximately €10.21 billion and FY25E revenues of €626 million (Exhibit 5), Technoprobe S.p.A. (TPRO) is a globally recognized leader in the semiconductor testing equipment industry, serving as a critical enabler for the chip manufacturing supply chain through the design and production of probe cards (see Annex 1).

Company presentation

Founded in 1996 by Giuseppe Crippa in Cernusco Lombardone, Italy, TPRO has evolved from a specialized entrepreneurial venture into a **multinational industrial group**.

The company successfully **listed** on Euronext Growth Milan in 2022 before transitioning to the regulated Euronext Milan market in **2023** to accelerate its international expansion and enhance institutional visibility. TPRO's core business focuses on **testing the functionality of complex non-memory (logic) chips** - such as CPUs, GPUs, SoCs, and AI accelerators - prior to packaging (the enclosure of a semiconductor chip in a protective case). By utilizing its proprietary Vertical MEMS (Micro-Electro-Mechanical Systems) technology, branded as TPEG™ (Technoprobe Proprietary Etching and Galvanic), the company has transitioned the role of the probe card from a standard consumable to a critical technological enabler.

TPRO maintains a highly centralized R&D and production hub in Italy, supported by a global service network spanning Silicon Valley and key Asian hubs. This technological leadership and geographical reach enable deep co-design collaboration with the industry's leading foundries (pure-play wafer manufacturers such as TSMC and GlobalFoundries), dominant fabless players (chip designers without manufacturing facilities, including Nvidia, Qualcomm, AMD, and Marvell), and IDMs (players combining both chip design and manufacturing capabilities, such as Intel, Samsung, NXP, STMicroelectronics, and Texas Instruments). To further strengthen its technological moat, TPRO has pursued a disciplined vertical integration strategy supported by targeted M&A activity. This approach has enabled inorganic growth (although limited) and progressively expanded the company's capabilities across critical segments of the semiconductor testing value chain. The company has also developed strategic partnerships with **Advantest and Teradyne**, leading ATE (Automated Test Equipment) manufacturers, enabling close alignment between the test machines and TPRO's probe cards, which must be custom-designed to operate seamlessly together (Exhibit 6).

Business Segmentation

TPRO operates through two complementary business lines: Wafer-Level Test (core business, accounting for ~80% of total revenues) and Final Test Solutions (~20% of revenues) (Exhibit 7, Annex 2).

Wafer-Level Test – Global Scale Player in a High-Complexity Market

TPRO is the second-largest global player in the Wafer-Level Test market, a structurally attractive and concentrated industry protected by high barriers to entry. The division designs and manufactures probe cards, utilized for functional and electrical verification at the wafer stage. Its technology portfolio includes TPEG™ Vertical MEMS, alongside Vertical and Cantilever probe cards, supporting a vast array of applications including Industrial & Automotive (11-13% of sales in FY25E), AI & Data Center (36-38% of sales) and Consumer (46-48% of sales). While consumer-end applications are exposed to cyclical semiconductor demand, overall volume is underpinned by structural drivers, such as increasing pin counts (the individual contact needles that interface with the chip during testing), shrinking pitches (finer pin distances), enhanced Current Carrying Capacity (CCC) and escalating thermal dissipation requirements. Operationally, the division is organized around its principal probe card technologies, with prototyping, engineering and manufacturing tailored to specific chip architectures and testing environments.

Final Test Solutions – Strategic Expansion into a Larger Downstream Market

TPRO's Final Test Solutions division represents the Group's expansion into downstream semiconductor verification, an adjacent market historically served by ATE vendors and specialized interface suppliers. Through the acquisition of DIS Tech, TPRO began focusing on the design of Device Interface Boards (DIBs), which, similar to probe cards in wafer testing, provide the physical and electrical interface between the test system and the semiconductor device during final electrical characterization.

Value and Cost Drivers

TPRO's core value proposition lies in its ability to integrate **advanced micro-fabrication with rapid customization** and scalable production, meeting the increasingly stringent demands of the semiconductor testing roadmap. As device architectures evolve toward (i) advanced nodes (7nm, 5nm, 3nm, and below), where smaller component sizes enable higher performance, lower power consumption, and greater functional density, (ii) advanced packaging, and (iii) AI-centric designs and high-precision probe cards have become mission-critical components.

TPRO mitigates time-to-market risks through a global footprint that includes **localized assembly, repair hubs** and on-site resident engineers at key customer facilities. This service model is underpinned by long-standing **co-development partnerships** with leading Fabless, Foundries, IDMs, and OSAT (Outsourced Semiconductor Assembly and Test) players. TPRO's advantage also lies in its ability to **optimize test reliability** by mitigating the costly trade-off between Type I errors (false rejects) and Type II errors (defective escapes). While the former directly erodes foundry yields and inflates the cost-per-good-die, the latter presents reputational risks for fabless designers who operate under a "zero-defect" mandate. TPRO's **Athena platform** serves as a safeguard against these inefficiencies. Athena minimizes the electrical noise that often triggers signal misinterpretation during high-speed testing. Furthermore, its high-density contact precision and mechanical stability under thermal stress enable the high parallelism necessary to compress delivery times.

The Group's business model necessitates sustained **investment in R&D** (~9.7% of Revenues in FY24), highly specialized engineering talent and the continuous automation of production facilities. In FY25E, TPRO allocated €50 million to **capital expenditures** (CapEx), primarily directed toward plant equipment and technological upgrades.

Corporate Strategy

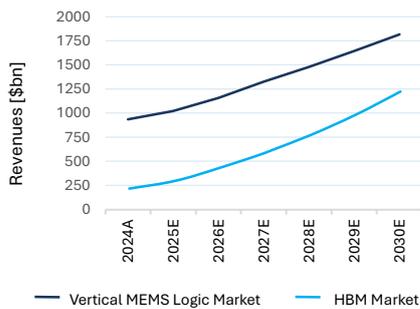
TPRO pursues a multi-pronged corporate strategy built on vertical integration, global footprint, and technology-driven growth (see Annex 6).

Vertical Integration & Partnerships

Technoprobe has historically pursued vertical integration, internalizing critical processes where technological advantages can be developed (see Annex 5). Its recent IPO signals intent to pursue larger, more transformative acquisitions. **Minor acquisitions** (Microfabrica, Yee Wei, MW Plasma) remain difficult to assess in value creation terms. In contrast, the **Harbor acquisition** (2023) failed to generate meaningful synergies, resulting in manufacturing footprint rationalization. In FY24, TPRO completed the \$85 million acquisition of **DIS Tech** from Teradyne, adding over 400 employees across multiple geographies and expanding design capabilities for high-performance Device Interface Boards (DIB). Notably, Teradyne simultaneously acquired a 10% equity stake, for about \$522 million, purchasing roughly 8% through newly issued shares and 2% from existing shares held by T-Plus S.p.A., followed by Advantest's acquisition of 2.5% stake in 2025.

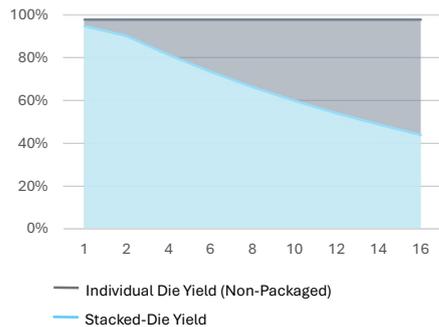
The minority **participation of two competing ATE vendors** underscores TPRO's strategic criticality as a neutral supplier within the semiconductor testing ecosystem, positioning the company to facilitate long-term collaboration frameworks for joint technology development.

HBM & Vertical MEMS: 5Y Market Roadmap – Exhibit 10



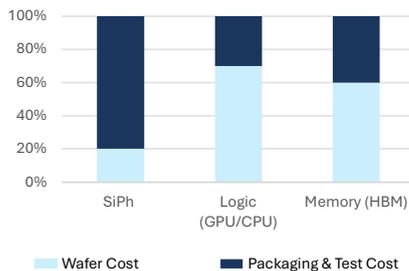
Source: Market Data, Team Elaboration

Chiplet Yield Gap, the value of KGD Test – Exhibit 11



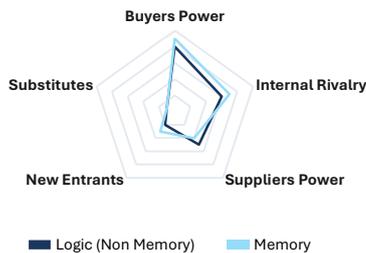
Source: Market Data, Team Elaboration

Cost Structure Comparison – Exhibit 12



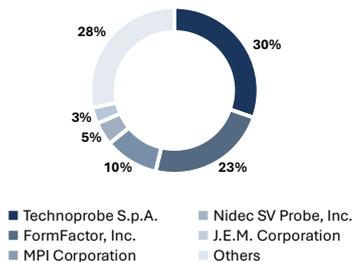
Source: Market Data

Logic: Porter's 5 Forces Analysis – Exhibit 13



Source: Team Elaboration

Market share logic – Exhibit 14



Source: Team Elaboration

Geographic Diversification

TPRO maintains approximately 3,355 employees (+1,700 in Italy) across **11 countries**, including **production plants, R&D centers, and sales offices** in Europe, Asia, and the U.S. This geographic presence enables TPRO to maintain physical proximity to major foundries, IDMs, and fabless customers, facilitating co-design, rapid customization, swift technical support and diversified end-market exposure. The Group's revenue distribution mirrors its global operational network, reflecting the geographic spread of its production, R&D, and sales activities worldwide (Exhibit 8).

Innovation as Competitive Lever

With over **600 patents and 7 dedicated research centers**, TPRO demonstrates strong commitment to technological leadership through sustained innovation investment. While each probe card is fully customized for specific chip architectures, TPRO has developed multiple platform families addressing distinct application segments: **(i) TPEG™ T40 and T50 technologies** enable minimal pitch scaling down to 40µm; **(ii) TPEG™ UXS90 and UXS70 platforms** focus on high density, high pin count applications with short, low-force needles; **(iii) TPEG™ T1/T1 HC (High Current)** solutions mitigate thermal stress during high-performance CPU and GPU testing under demanding power requirements; **(iv) TPEG™ V-Mantis technology** delivers elevated operating temperatures and high mechanical force capability; and finally **(v) Phantom and Ultra Phantom platforms**, leveraging proprietary SRF (Shield Radio-Frequency) technology, achieve ultra-high GHz performance while maintaining low cross-talk and leakage characteristics.

Industry Overview

The semiconductor probe card market is defined by a **sharp contrast in growth dynamics**: while the established Logic segment shows steady expansion with an 6.95% CAGR 2025-2030, the Memory sector (encompassing HBM) is surging with a 15.27% CAGR 2025-2030 (Exhibit 9).

Regarding the final testing market, it is projected to expand at a 7.9% CAGR from 2025 to 2030. This industry involves complex competitive dynamics, with incumbents facing pressure from shortened chip development cycles, now reduced to just 1.5-2 years, and from an unbalanced relationship between large customers and small testing companies. Beyond these baseline dynamics, several transformative trends are reshaping the testing landscape for 2025 and the subsequent years.

Industry Trends

(i) THE CHIPLET REVOLUTION. The semiconductor industry is transitioning from monolithic System-on-Chips, where all functions are integrated on a single die (an individual silicon unit containing an integrated circuit), toward modular chiplet-based architectures. This shift reflects physical and economic limits in chip manufacturing, as larger dies suffer disproportionately from yield losses. Chiplet designs mitigate this risk by splitting complex chips into smaller, function-specific dies that are manufactured and tested separately before being assembled into a single system. This architectural shift materially increases the importance of early-stage testing. In chiplet-based designs, a defect in any individual die can compromise the entire high-value package, requiring each chiplet to be tested and certified as a Known Good Die (KGD) prior to assembly.

(ii) HYPER-SCALING OF AI INTERFACES. To meet the massive data throughput demands of generative AI, chip-to-chip interfaces are moving to significantly higher signaling speeds. At these rates, the physical path between the tester and the silicon die becomes the primary source of signal degradation, rendering traditional probe cards insufficient. Reliable testing therefore requires radio-frequency (RF) probe technologies, engineered to preserve signal integrity across the entire path from tester to die. Importantly, this shift toward RF probing should be viewed not as the emergence of a new or disruptive market, but rather as a necessary technological evolution that supports the higher-performance requirements driven by HBM and advanced AI architectures, enabling existing test paradigms to scale rather than fundamentally changing them.

(iii) HIGH BANDWIDTH MEMORY (HBM) EXPLOSION. High-Bandwidth Memory (HBM) has emerged as a key constraint in the scaling of AI accelerators, as system performance increasingly depends on memory bandwidth rather than compute alone. Driven by AI workloads, **HBM revenue is projected to grow at a 33% CAGR through 2030 (Exhibit 10)**. Modern HBM architectures stack **12-16 individual memory dies**, creating a near zero-tolerance environment for defects, where a single faulty component can compromise an entire high-value stack (Exhibit 11). To mitigate this risk, manufacturers rely on rigorous die-level and wafer-level testing to ensure that only fully verified components are assembled, enabling the concept of a "Known Good Stack" (KGS).

This evolution is driving new probing architectures, including **Direct Attach** and **Direct-to-Die**, which bypass conventional package substrates to minimize signal loss, one of the key challenges of the "Terabit Era" project. As HBM architectures become denser, traditional micro-cantilever probe cards reach their physical limits, driving a transition toward **Vertical MEMS architectures** that enable high-precision verification of dies prior to stacking.

(iv) SILICON PHOTONICS (SiPh) INTEGRATION. As copper interconnects approach physical and energy-efficiency limits, data centers are increasingly adopting **Silicon Photonics (SiPh)** and **Co-Packaged Optics (CPO)** to support higher data rates and lower power consumption (Exhibit 12). Silicon photonics integrates optical components - used to transmit data as light - alongside electronic circuits, enabling faster and more energy-efficient communication than traditional copper-based links.

Given the fundamental size constraints of optical components, the industry is converging toward **hybrid packaging architectures**, in which photonic chips are integrated with electronic dies within the same package. This transition introduces a **new testing paradigm**, requiring the **simultaneous validation of optical and electrical performance** with sub-micron alignment precision.

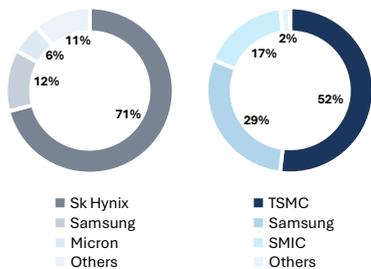
TPRO Positioning

TPRO's core business is firmly rooted in the high-tech semiconductor ecosystem through its advanced portfolio of MEMS probe cards. While the company has established a solid position in the Logic testing segment, its exposure to faster-growing AI applications (see Annex 3) remains at an early stage. Progress in these areas is subject to **execution risk, uncertain adoption timelines**, and an **increasingly competitive landscape**, which together represent key sources of uncertainty for the investment case.

(i) CHIPLET REVOLUTION. TPRO is strategically positioning itself to capitalize on the Advanced Packaging surge, identifying chiplet testing as a primary enabler for the industry. While advanced packaging offers significant performance gains, it introduces the risk of **compounded yield loss**; as the number of integrated dies increases, any defect leads to an exponential surge in scrap costs for high-value assemblies. To mitigate this, TPRO addresses four fundamental technical bottlenecks: **(i) It manages fine-pitch and ultra-high pin count requirements** essential for HPC (High-Performance Computing) through precision MEMS scaling; **(ii) It optimizes high-speed performance** by leveraging short-needle architectures and **(iii) handles high power delivery and thermal constraints** via active cooling; **(iv) It enables high-density interconnections** through advanced MLO (Multi-Layer Organic), ensuring a seamless interconnectivity between the micro-scale die and the macro-scale tester.

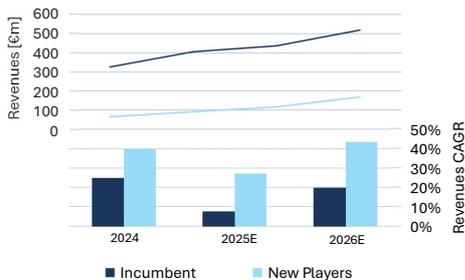
(ii) HYPER-SCALING OF AI INTERFACES. TPRO has deployed advanced RF technologies to address the exponential surge in data transfer speed requirements. To this end, the company has developed two proprietary solutions:

Customer Concentration (Logic, Memory) – Exhibit 15



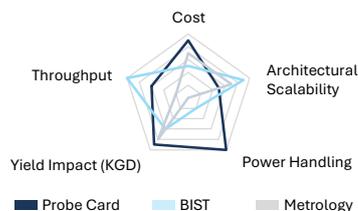
Source: Market Data

New Players vs. Incumbent Growth – Exhibit 16



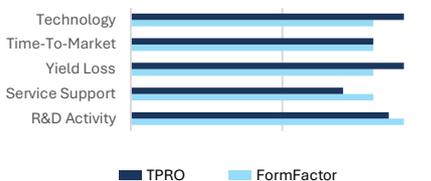
Source: Market Data

Probe Cards, BIST, Metrology Technical Capability Gap – Exhibit 17



Source: Team Elaboration

The Global Probe Card Duopoly – Exhibit 18



Source: Team Elaboration

SWOT analysis – Exhibit 19

STRENGTHS

- Dominant Non-Memory testing position
- Strong R&D heritage
- Strategic partnerships
- High liquidity

WEAKNESSES

- High customer concentration
- Limited product diversification
- Margin dilution
- Workforce scarcity
- Capacity Constraint

OPPORTUNITIES

- Expansion into Memory market
- New customer acquisition in AI
- M&A opportunities
- Transfer of tech leadership to different segments

THREATS

- Supply chain vulnerability
- Rapid tech obsolescence
- Talent shortage
- Competition from larger players

Source: Team Elaboration

Phantom and UltraPhantom. Notably, TPRO has demonstrated that its UltraPhantom (UP) technology can support frequencies up to **150 GHz at a 100 μm pitch** (the distance between two consecutive probes), effectively covering the bandwidth required for next-generation AI interfaces.

However, despite the strong technical specifications, UP may not ultimately represent a clear game changer, as competing solutions with comparable performance are already being developed by other industry players.

(iii) HIGH BANDWIDTH MEMORY (HBM). Challenges in the HBM testing market remain significant, as TPRO’s success is contingent on **customers deciding to adopt next-generation memory technologies**, which would create demand for the company’s solutions. Securing qualifications from the ‘Big Three’ memory foundries (SK Hynix, Micron, and Samsung) is essential to meet these requirements, and TPRO has already secured one of these players as a customer (likely Samsung, based on the fact that Samsung is already a TPRO customer in the logic segment). The segment is further complicated by **strong incumbents with established relationships**, such as FormFactor and MJC, which create high barriers to entry. With adoption of HBM4e and HBM5 still in **early stages**, the potential industry-wide shift to Vertical MEMS could provide an opportunity for TPRO in 2028 to penetrate this segment (we estimate 15-20% market share), although the timing and scale of such a transition remain uncertain (*Annex 3*).

(iv) SILICON PHOTONICS (SiPh). TPRO’s Eclipse Dynamic probe card appears to technically leapfrog competing solutions by integrating **automated fiber alignment** directly on the card, which precisely positions optical fibers to maximize light transmission to and from the device. The adoption of on-card optical alignment remains at a very early stage, with limited visibility on whether it will ultimately emerge as the prevailing industry standard as production scales to high volumes. Market leadership is currently contested by a **broad set of players**, some of which are exclusively focused on this specific application and may therefore benefit from greater specialization and earlier customer engagement. In addition, **Chinese competitors** appear to be pursuing an increasingly aggressive market entry strategy, potentially intensifying price competition and accelerating technological convergence.

Porter’s Five Forces

Overall industry attractiveness (*Exhibit 13*) is strongly supported by high technological barriers to entry, which limit competitive pressure, and a structural shift toward high-growth segments such as AI-driven memory.

(i) Internal rivalry varies by segment but remains a significant factor in determining attractiveness. The **Logic segment** is moderately concentrated (HHI=1,604), characterized by a balance between global leaders like TPRO (30.3% share), **FormFactor** (23.3%) and **MPI** (10.4%). Conversely, the **Memory segment** exhibits higher concentration (HHI=2,098) and more intense rivalry among a narrower group of incumbents, including **MJC** (35.3%) FormFactor (27.0%) and **JEM** (11.3%) (*Exhibit 14*). Within the high-growth HBM sub-segment, TPRO is poised to emerge as a potential challenger to established Japanese and U.S. incumbents, aiming to capture AI-driven demand.

(ii) Buyer power is structurally high, as TPRO’s **top three clients** account for **~59% of revenues** (*Exhibit 4*) and are global chip players whose scale and negotiating leverage far exceed TPRO’s. While the company’s proprietary TPEG™ Vertical MEMS platform and 600+ patents provide a technological edge, revenue growth is constrained by this **concentrated customer base**, exposure to semiconductor market cycles, and the increasing commoditization of probe card technologies, particularly in the low-end segment. (*Exhibit 15*).

(iii) Supplier power is moderate, as TPRO leverages **deep vertical integration** to insulate its operating margins from supply chain volatility, having effectively internalized nearly all high-value manufacturing steps. The company remains strategically dependent on third parties for the **PCB components** within the probe card, **supplied by partners** including **Advantest and Teradyne** (see *Annex 2* for details on the probe card architecture and components). Lastly, vulnerability to precious metal procurement remains low due to the limited volumes required.

(iv) The threat of new entrants is overall medium-low due to formidable “IP Walls” and extreme capital requirements. A greenfield MEMS facility requires upwards of \$150 million in investment, alongside a 18 month qualification void that prevents swift market penetration. Furthermore, the necessity for “Resident Engineers” and local repair infrastructures creates an operational moat; new entrants cannot easily replicate the deep integration incumbents have with giants like TSMC or SK Hynix. Nevertheless, emerging competitors – particularly Asian players – are gaining traction by leveraging their established relationships with major chipmakers (*Exhibit 16*).

(v) Substitute threats remain low as physical contact remains indispensable for functional validation (*Exhibit 17*). While contactless technologies optimize size, they cannot replace physical probing for full electrical characterization.

Competitive Positioning

The global probe card market is highly concentrated: TPRO commands a dominant 60% market share in Vertical MEMS Logic testing, largely by leveraging its proprietary TPEG™ Vertical MEMS architecture.

This position is further reinforced by an **agile operating model** that shortens development cycles by around 20%, as clients are facing faster development cycles. However, the company’s investment profile faces headwinds from a highly concentrated portfolio, a underperforming M&A track record and a management structure still transitioning toward global institutional standards. A comparative analysis across five key drivers - **technology, time-to-market, yield, service, and R&D** - shows that TPRO and Form Factor are fighting a close battle in the industry (*Exhibit 18*).

In terms of technology, TPRO has potential in RF, SiPh, and high-end Logic applications, specifically for GPUs and CPUs. Its time-to-market remains highly competitive with industry peers, maintaining a three-week prototyping and four-week production cycle. Regarding reliability, we estimate a yield of 98-99%, with a guaranteed durability of over one million touchdowns; however, the total component lifespan currently trails FormFactor’s benchmarks.

Looking ahead, TPRO might position itself as a challenger in the HBM space, where U.S. and Japanese incumbents currently hold a first-mover advantage. This potential role depends on customers opting to adopt TPRO’s TPEG™ Vertical MEMS platform for testing next-generation memory devices.

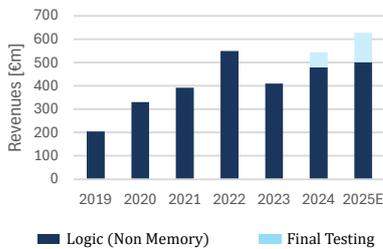
SWOT Analysis

The segment in which TPRO operates is rapidly evolving, with smaller players developing quickly and the ability to continuously adapt being critical (*Exhibit 19*). Despite **strong patent protection** supporting its ongoing R&D, the company remains exposed to copycats. Agreements with partners such as WinWay reduce the incentive to replicate TPRO’s technology: authorizing them to sell its products, the Group effectively expands the market reach of its products. At the same time, TPRO faces increasing pricing and performance pressure from Tier-1 customers, which leverage their scale to negotiate more favourable terms.

TPRO’s **€657 million cash position** provides a strong foundation for portfolio diversification and deeper vertical integration via M&A and R&D, but these initiatives involve meaningful trade-offs. Aggressive expansion has already led to **operating margin dilution**, signalling a shift toward a riskier profile. Execution risk is further heightened by plans to double production capacity within two years. In 2025, capacity utilization is already close to saturation, at around 90%, which constrains near-term expansion despite potentially strong demand. As a result, capacity additions appear necessary to support growth; however, given the inherent cyclicality of the semiconductor market, this strategy also carries the risk of overcapacity should demand normalize or weaken (*Annex 11*). As TPRO enters the **HBM segment**, it faces a “two-front war”: defending its core logic franchise from incumbents encroaching on its strongholds, while simultaneously challenging established leaders in memory. As a result, long-term valuation depends on TPRO’s ability to penetrate the HBM market and leverage its **Vertical MEMS leadership** into a durable competitive advantage in memory testing.

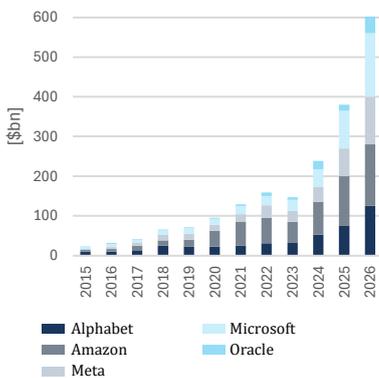
Financial Analysis

Historical Revenues Breakdown by Segment – Exhibit 20



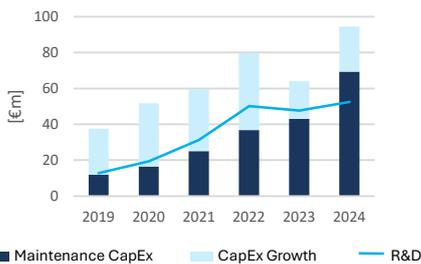
Source: Team Elaboration, Company Data

CapEx of Hyperscalers – Exhibit 21



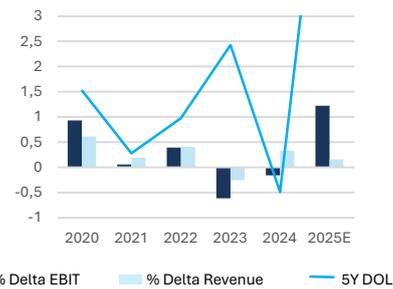
Source: Team Elaboration, Company Data

CapEx, R&D Expenditure – Exhibit 22



Source: Team Elaboration, Company Data

5 Years Degree of Operating Leverage (DOL) – Exhibit 23



Source: Team Elaboration, Company Data

Revenues vs. EBITDA margin – Exhibit 24



Source: Team Elaboration, Company Data

Historical Analysis

REVENUES

TPRO has delivered a **strong revenue expansion** over FY19-FY24 (22% CAGR), primarily supported by the structural increase in semiconductor device complexity. Revenues reached €543m in FY24, broadly in line with the FY22 peak, which was **inflated by extraordinary consumer-driven semiconductor demand** during the COVID period. Following a post-pandemic contraction in FY23 (-25% Rev vs FY22), growth resumed in FY24, supported by the consolidation of the DIS Tech business (Final Testing, *Exhibit 20*). TPRO's revenue profile remains characterized by elevated customer concentration: with top three customers consistently accounting for a significant share of total revenues, peaking at 58% in FY22 at the height of the semiconductor upcycle and remaining structurally around that level through FY25E (*Exhibit 15*).

A global reality: from a geographic standpoint, Italy and the rest of Europe remain marginal end markets (*Exhibit 9*), jointly contributing less than 7% of FY24 revenues. Sales generation is highly concentrated in Asia (46.8%) and U.S. (46.1%), highlighting TPRO's pronounced sensitivity to global foundries and Hyperscalers CapEx cycles (*Exhibit 21*).

MARGINS

TPRO has historically delivered **best-in-class profitability**, supported by a strong **operating leverage** which enabled effective cost absorption (see *Annex 11*). Over FY19-22, the Company consistently reported Gross margins of approximately 65% and EBITDA margins around 45%, despite rising operating expenses related to capacity expansion and R&D investments (*Exhibit 22*).

However, all that glitters is not gold: while operating leverage supported earnings during the upcycle (1.0x DOL FY22; *Exhibit 23*), it also amplified the subsequent downturn, with EBIT declining more sharply than revenues in FY23 (2.4x DOL). As a result, profitability materially deteriorated in FY23, with Gross margin decreasing to 56% (vs 65% in FY22) and EBITDA margin compressing to approximately 30% (vs 45% in FY22, *Exhibit 24*). The sector-wide downturn led to a **sharp contraction in volumes**, limiting operating leverage, while management's decision to maintain headcount and productive capacity throughout the period further constrained margin recovery. Foreign exchange exposure also contributed to margin pressure: the Group generates 90% of its revenues in USD, while a significant portion (around 80%) of its costs is euro-denominated, creating a natural currency mismatch. In FY24, despite a strong top-line recovery (+33% revenues YoY), **profitability failed** to normalize with **EBITDA margin declining to 25%**, reflecting the dilutive impact of DIS Tech consolidation, whose structurally lower margin profile (16% Gross margin FY24) weighed on Group profitability.

Margins are only one part of the story: the assessment of returns on invested capital is essential to evaluate how efficiently the company deploys its resources. **ROIC** ex-goodwill sharply deteriorated following the FY20-22 upcycle, declining from 47% in FY22 to just 8% in FY24 (*Exhibit 25*). That said, a partial recovery is expected in FY25 (17% ROIC), supported by improving revenues and margin enhancement driven by the optimization of DIS Tech activities.

CAPEX, D&A, INTANGIBLE

Investing to survive: over FY19-24, TPRO consistently executed a disciplined, **capital-intensive investment strategy** aimed at supporting long-term growth and technological development. As a result, CapEx remained structurally elevated, representing ~14-18% of revenues, with investment levels holding steady even during the FY23 semiconductor downturn, reflecting management's **commitment to maintain spending** despite challenging market conditions. This commitment is confirmed by CapEx/D&A ratio throughout the period (avg of 2x between FY19-24), which highlights a sustained and intensive investment cycle. Consistent with this trajectory, **R&D expenditure faced a constant acceleration**, resulting in an increase in intensity from 6.3% of revenues in FY19 to 9.7% in FY24, fully in line with the one in the sector (*Exhibit 26*).

Finalizing the Strategic Picture: TPRO's growing investment in intangibles highlights its commitment to long-term value creation and reinforces its capital allocation strategy. **Intangible assets increased sharply** in FY24 (+266% YoY) mainly attributable to the consolidation of the DIS Tech business, with intangibles over revenues also rising materially (12% in FY24 vs 4% in FY23). At the same time, goodwill represents only 3.7% of equity in FY24, indicating that TPRO's growth has been primarily driven by organic investments and disciplined, targeted acquisitions rather than balance-sheet-intensive M&A.

FOCUS ON M&A

Shade and Lights: TPRO has relied on M&A (5 acquisitions since 2019) to complement its growth strategy, using acquisitions mainly to **strengthen know-how**, vertical integration and drive strategic consolidation **rather than** to accelerate **revenue growth**. Despite limited disclosure on transaction values, we estimate that TPRO paid less than 1x historical Revenues (see *Annex 5*) with a significant positive impact on know-how generated (130% avg intangible increase FY22-25). Since 2019, TPRO has spent approximately **€190m on acquisitions**, which contributed around €72m in revenues in the consolidation years, suggesting a **disciplined and technology-driven approach** to inorganic growth, focused on long-term value creation rather than short-term revenue expansion. While some acquisitions, such as **Microfabrica**, successfully enhanced TPRO's manufacturing capabilities, others failed to deliver the expected benefits. **Harbor Electronics**, acquired in 2023 to integrate PCB supply, **faceted operational inefficiencies** (€792k Net losses FY23), leading to the shutdown of U.S. manufacturing operations in 2025 (while transferring its know-how to TPRO's core business). Furthermore, **DIS Tech** transaction led to **short-term margin dilution**, (15% EBITDA margin FY25E) and came at the cost of 10% equity dilution and a Board seat for Teradyne's CEO, granting Teradyne more influence despite its diminishing strategic appeal, as the firm currently lags in the AI application segment.

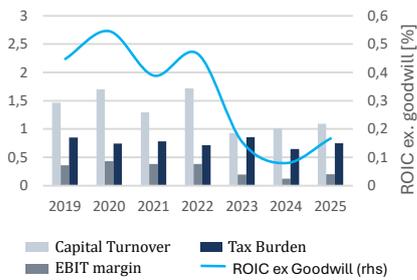
Future Expectation: given the largely vertically integrated nature of TPRO's probe card business, we expect future **M&A activity to remain selective and strategic**, leveraging on strong cash position. Potential targets are likely to include bolt-on acquisitions at slightly higher multiples (1.5-2x Revenues) aimed at enhancing manufacturing processes, as well as developing disruptive technologies, including SiPh and Radio Frequencies.

LIQUIDITY ANALYSIS

If cash is King, TPRO runs the treasury: with a strong net financial position of - **€656m** in FY24, supported by the 8% capital increase with Teradyne (€385m), and an average FCF margin of 12% over FY19-25E, cash generation does not represent a constraint (123% cash and cash equivalents on Revenues). Robust free cash flows have supported business growth ambitions, while sustaining elevated CapEx and R&D investments (17% and 9.7% of sales in FY24, respectively). This position results in a **minimal reliance on debt financing**, reflecting the Crippa family's reluctance to employ leverage: the average D/E in FY19-25E stands at 2.9%, with an interest coverage ratio surpassing 43x in FY24. However, the group's conservative leverage profile offers no multiplier effect on ROE, which declined from an average of 25% in FY19-22 to 8% in FY23-25E, representing a significant headwind for shareholder value creation.

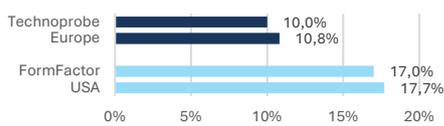
A king without the crown: TPRO exhibits relatively **limited bargaining power**, as reflected in a persistently **extended cash conversion cycle**, which reached 146 days in FY25E (*Exhibit 27*), mainly driven by elevated days inventory outstanding. Inventories increased to an average of 31% of Revenues in FY23-24 from 15% in FY19-22, reflecting inventory build-up ahead of expected AI-driven demand. As a result, working capital intensity remains structurally high

DuPont Analysis – Exhibit 25



Source: Team Elaboration, Company Data

R&D expenditure/Sales vs. main competitor – Exhibit 26



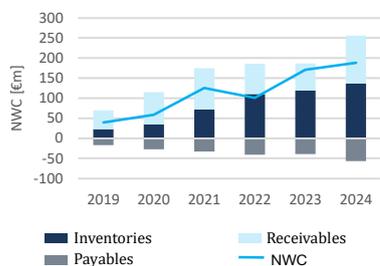
Source: Team Elaboration, Company Data

Cash Conversion Cycle – Exhibit 27



Source: Team Elaboration, Company Data

Net Working Capital – Exhibit 28



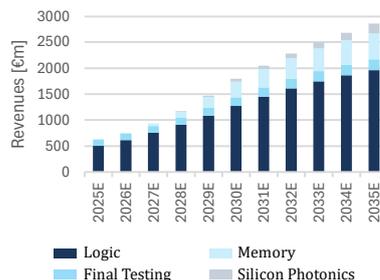
Source: Team Elaboration, Company Data

Peers 2024A EBITDA margin comparison – Exhibit 29



Source: Team Elaboration, Market Data

Expected Revenues – Exhibit 30



Source: Team Elaboration, Company Data

and volatile, with the net working capital-to-revenue ratio consistently above 30% over FY21-FY24 and peaking above 40% in FY23. Elevated receivables and inventory accumulation have led to significant capital absorption and structurally weaker cash flow conversion (Exhibit 28).

COMPETITIVE FINANCIAL ANALYSIS

A giant in the niche: TPRO has benefited from revenue growth driven by both **volume expansion** and **market share gains**, leaving limited room for competitors. Over FY19-24, TPRO delivered the **strongest growth in the segment**, with a 22% revenue CAGR, materially outperforming FORM (5.3%) and the broader peer average (9.5%). This performance confirms an aggressive investment strategy. While TPRO's R&D intensity (9.7% of revenues in FY24) is **broadly in line** with peers but below FORM (17%), the Group differentiates itself through materially higher capital intensity. CapEx reached 17.6% of revenues in FY24, **significantly above FORM** (5%) and the peer average (10%), with CapEx/D&A consistently above 1x, underscoring an expansionary capital allocation stance. Moreover, TPRO's profitability remains consistently in line with the segment average and materially above FORM (FY24: 25.1% vs 17.2%), reflecting **stronger operating leverage** (Exhibit 29). By contrast, working capital dynamics point to **weaker commercial positioning**. TPRO exhibits a structurally longer cash conversion cycle than FORM (146 days vs 84 days in FY25), mainly driven by higher DIO, consistent with a more conservative inventory policy.

Forecast Analysis and Valuation Assumptions

REVENUES

Growing at a slow pace: the FY25 outlook appears positive at first glance, with revenues expected to grow by 15.4% YoY. However, this increase is largely driven by the first full-year consolidation of DIS Tech; organic growth in the Logic segment is limited to a modest 4.6%, pointing to a weak performance of the core business.

Recovery in the future: looking beyond 2025, we expect TPRO's financial performance to be primarily influenced by: (i) strong growth in the **Logic** segment, driven by AI-related GPU demand; (ii) the contribution of the **Final Test** segment, which is expected to grow linearly; (iii) **HBM** market entry, though with a revenue contribution that remains uncertain in terms of both timing and magnitude; and (iv) the new **SiPh** segment, which is forecasted to impact revenues from 2028 onwards. Consequently, we forecast double-digit growth, with a FY25E-28E CAGR of 23.2% (Exhibit 30), representing a 420 bps discount to consensus (27.4%, FactSet). In the outer years, we assume a normalization, with a FY28E-35E CAGR of 13.6%.

Logic Revenues forecast: To estimate revenues in the core Logic segment over FY25-28, we analyzed the historical relationship between TPRO's Revenues and **TSMC's wafer production**, reflecting TSMC's role as TPRO's main customer and its 70% share of global logic chip production. This choice is supported by a clear economic linkage: beyond being the Company's largest direct customer, probe cards sold to fabless clients are often ultimately deployed at TSMC, implying that the Foundry captures a broader share of TPRO's effective demand than suggested by direct revenues alone (32.1% in FY25E). The analysis shows a strong correlation between the two variables (0.87), and a regression analysis confirms a statistically significant beta, supporting the use of TSMC wafer output as a reliable proxy for demand trends of TPRO. Based on these dynamics, we assume a **FY25-28E CAGR of 21%** for the Logic segment, resulting in FY28E revenues of €907m. For FY29-30, we assume a moderation in growth rates to reflect cyclical and normalization in the Logic market (18.5% CAGR).

Final Testing: For the Final Test segment, we adopt a **linear and conservative** modelling approach. Despite a reference market CAGR of 7.4%, we believe the structurally lower margin profile of the business and the already failed vertical integration plan (Harbour) limits incentives for capacity expansion. Accordingly, we assume that TPRO will invest primarily to **maintain** its current market position (no material market share gains), with revenues growing broadly in line with the market reaching €164m by FY30E.

HBM: To model revenues from the HBM market over FY25-30, we adopt a **top-down approach**. The Memory market is expected to grow at a 15.3% CAGR, largely driven by the adoption of HBM solutions in GPUs. We therefore attribute market growth primarily to HBM, while the broader Memory segment (NAND and conventional DRAM) is projected to grow at a 6% CAGR.

TPRO's qualification at a leading Memory manufacturer (likely Samsung, given their existing relationship in Logic) could pave the way for future certifications at Micron and SK Hynix. However, qualification alone does not guarantee Revenue conversion. Significant growth hinges on a technological transition to Vertical MEMS, a development with uncertain commercial timelines. Therefore, we model a **gradual ramp-up**, resulting in a 20% market penetration in 2028 (€113m Revenue FY28E). From 2028 onwards, we assume TPRO's market share rising from 20% to 35% of TAM, with FORM still expected to be the segment's leader.

SiPh: Starting from 2028, we expect TPRO to enter the Silicon Photonics (SiPh) market through a gradual and cautious ramp-up, consistent with the Group's historical approach to high-innovation segments. Accordingly, the initial revenue contribution is expected to be limited (€9m FY28), **with a progressive acceleration** from 2030 onwards supported by technology maturation and broader customer adoption. Revenue projections follow a **market-based methodology**: the addressable market is derived by applying the estimated probe card penetration within the projected total SiPh market, assumed to grow at a 30% CAGR over FY28-32. TPRO's segment revenues are then estimated assuming a 30% market share, consistent with our expectations for TPRO's advanced ECLIPSE solution.

CAPEX AND D&A

Capacity expansion: We assume incremental CapEx of **€150m over FY26-27** to support TPRO's transition to a structurally higher growth phase, primarily aimed at expanding manufacturing capacity for rising Logic & HBM driven demand. The additional CapEx is not equally distributed across the two years, with **~€57m in FY26** and **€93m in FY27**, reflecting a progressive ramp-up in capacity-related investments. The incremental CapEx is primarily allocated to: (i) production facilities (~30%); (ii) **high-precision manufacturing equipment (~60%)**; and (iii) other production and support assets (~10%). This extraordinary investment layer is assumed in addition to recurring maintenance and innovation CapEx (€50m) required to support **ongoing technological upgrading** and operational competitiveness. As a result, during the ongoing capacity expansion phase, total CapEx is estimated at €107m in FY26 and €143m in FY27. From FY28 onwards, we assume a slow down of Capex with another peak in FY30-2031 to support further plant expansion in line with expected demand growth. All these considerations result in an avg. CapEx-to-Revenues ratio of 6.5% over FY28-FY35.

Depreciation and amortisation are modeled to grow at a slower pace than CapEx. For FY26-28, D&A are estimated on a bottom-up basis starting from FY25 H1 financials. Beyond FY28, we apply the historical average, corresponding to 5% of revenues, resulting in D&A remaining structurally below projected CapEx (avg. D&A/CapEx of 0,8x). In the terminal year, we assume a CapEx/D&A ratio of 1.1x, consistent with a stable long-term growth profile.

MARGINS

Stability in Profitability: Regarding profitability, starting from management guidance for the first two forecast years (FY26-27), we have increased the Company's EBITDA margin assumptions by 200 bps, bringing them to 40% and 42%, respectively. This uplift is supported by our analysis of the plant closure of two U.S. facilities (Harbor Electronics and Microfabrica) and by the expectation of sustained high utilization rates of Italian plants (above 90%). In FY28 we assume a **margin compression of approximately 400 bps**, driven by a combination of operational factors: (i) **ramp-**

DCF Stages Data – Exhibit 31

	First Stage	Second Stage	Terminal Value
Years	2025E-30E	2030E-35E	>2035E
Sales CAGR	19%	10%	4%
Avg. EBITm	32%	37%	37%
% on EV	9%	17%	74%

Source: Team Elaboration, Company Data

WACC Computation – Exhibit 32

WACC = 9.21%		
Risk Free Rate (Rf)	2.89%	Current 10-y German government bond yield
Equity Risk Premium (ERP)	4.77%	Equity risk premium derived from Damodaran ERP implied, adjusted for country risk of USA, Europe, Taiwan, South Korea
Beta (β)	1.33	Estimated by leveraging the peers median unlevered beta to TPRO's capital structure
Cost of Equity (Ke)	9.21	Capital Asset Pricing Model $K_e = R_f + \beta * MP$
Cost of Debt (Kd)	0%	Due to debt-free capital structure; WACC equals the cost of equity
Tax Rate	25%	Debt tax shield is reflected through the application of a corporate tax rate on earnings before taxes
Leverage (D/E)	1.5%	Current leverage, no potential upside due to Governance decisions

Source: Team Elaboration, Company Data

Montecarlo Analysis – Exhibit 33



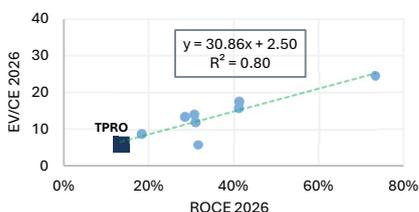
Source: Team Elaboration

Bull vs. Bear Scenario – Exhibit 34



Source: Team Elaboration

EV/CE 2026E regressed against ROCE26 – Exhibit 35



Source: Team Elaboration

up costs associated with the new production capacity; (ii) entry into the **HBM segment**, which carries **lower margins** relative to Logic; and (iii) **sub-optimal utilization rates** of installed capacity during the initial expansion phase. Over the FY29-35 period, we assume broadly stable EBITDA margins around 42%, with a slight temporary decline in FY31 driven by the expansion of production facilities, before returning to normalized levels.

	2024	2025E	2026E	2027E	2028E	2029E	2030E	2031E	2032E	2033E	2034E	2035E
Revenues [€m]	543	626	754	947	1,172	1,466	1,792	2,049	2,283	2,494	2,684	2,857
Growth YoY	32.7%	15.4%	20.4%	25.6%	23.8%	25.1%	22.3%	14.3%	11.4%	9.2%	7.6%	6.5%
Logic growth	17.1%	4.7%	22.8%	22.5%	20.2%	19.1%	18.0%	14.0%	10.9%	8.5%	6.6%	5.1%
Final Test growth	-	95.3%	-1.2%	7.4%	7.4%	7.2%	7.2%	6.7%	6.0%	5.4%	4.9%	4.4%
Memory growth	-	-	-	233.0%	89.1%	86.4%	43.4%	17.1%	12.8%	9.6%	7.2%	5.4%
SiPh growth	-	-	-	-	-	137.1%	137.1%	30.1%	29.8%	29.8%	29.2%	28.7%
EBITDA [€m]	136	217	301	397	445	586	753	840	959	1,0725	1,1541	1,228
EBITDAm	25%	35%	40%	42%	38%	40%	42%	41%	42%	43%	43%	43%
EBIT [€m]	671	148	231	323	359	498	663	745	846	957	1,037	1,109
EBITm	12.4%	23.8%	30.7%	34.2%	30.7%	34.0%	37.0%	36.4%	37.1%	38.4%	38.7%	38.8%
Net Profit [€m]	62	111	173	24	269	374	497	558	635	718	777	832
NPm	12%	18%	23%	26%	23%	26%	28%	27%	28%	29%	29%	29%
FCFF [€m]	21	106	100	118	197	281	340	391	557	647	713	771
CapEx	94	50	107	143	94	96	153	189	123	125	128	130
NFP [€m]	(655)	(704)	(743)	(780)	(881)	(1,037)	(1,216)	(1,425)	(1,776)	(2,194)	(2,660)	(3,167)
ROCE	8%	17%	27%	33%	33%	41%	48%	47%	48%	51%	53%	54%
ROE	5%	8%	13%	15%	15%	18%	20%	19%	18%	18%	16%	15%

Valuation

We initiate our coverage on TPRO with a **HOLD recommendation** and a year-end TP of €15.38 per share, implying a -1.6% downside from 31st January 2026 price (€15.63 per share). Our valuation is based on an asset-side DCF model, best suited to capture (i) the uniqueness of Vertical MEMS business model and (ii) the Company's current transition phase, as described in *Forecasted analysis and valuation assumptions*. To sustain and assess the soundness of our assumptions, we complemented the DCF with (i) a **Montecarlo simulation** and (ii) a **market-based relative valuation**, resulting in a €15.83, fully aligned with our year-end target price.

Discounted Cash Flow (DCF)

We performed a three-stage DCF (*Exhibit 31*) based on a 9.21% WACC (*Exhibit 32*), capturing (i) the expansion of its activities until 2030, (ii) a fade-out phase marked by decelerating revenue growth, and (iii) a terminal value derived through a perpetuity with a 4% terminal growth rate. FCFs are explicitly forecast over FY25E-35E.

2025-2030: Fuelling the AI Scale-up. In the first stage, according to our forecast presented in the *Forecast analysis*, we predict a 19.15% revenue CAGR, reflecting TPRO's **exposure to the AI scale-up** as a key player, through the entrance in the HBM and SiPh segment, and the **strong positioning in the Logic segment**. In the short-term (FY26-27), we considered a growing level of CapEx (69% CAGR FY25E-27E) to support capacity expansion, leveraging on high cash availability. In the medium-long term, we expect (i) best-in-class EBITDA margin of 40%, but lower than FY19-22 cycle due to margin dilution from the **HBM business and capacity expansion**; and (ii) market share gain in memory and silicon photonics market (30% in both segment from current zero), driven by technological competitive advantage.

2031-2035: Reaching the maturity. In the second stage, we assume a **phase of consolidation** following the expansion peak. During this phase, the Company is expected to benefit from (i) sustained revenues growth (9.77% CAGR in FY31E-2035E), (ii) higher profitability supported by improved operating leverage (EBITDA margin 43%) and (iii) a normalized CapEx intensity (CapEx/Revenues 5.7%).

Terminal Value. In the final stage, the terminal value is derived using the perpetuity approach based on FCF of FY35E, assuming a 4% long-term growth and a 9.21% WACC. TPRO is expected to benefit from (i) a heavy presence in the Logic and HBM segment, and (ii) a readiness to compete with the next-generation technologies as the SiPh.

Montecarlo Analysis

To stress-test our assumptions, we performed a Monte Carlo simulation (*Exhibit 33*) **across 10,000 scenarios** (see *Annex 8*), varying the most critical parameters of our valuation model: (i) WACC, (ii) Terminal Growth Rate, and (iii) Revenue YoY Growth. The latter was dynamically linked to the EBITDA margin using an operating leverage model. Our HOLD recommendation is well-supported, with the **current valuation falling within the fair value range** in the vast majority of simulated cases (*Exhibit 34*), precisely 75%.

Relative Valuation

Relative valuation was performed to cross-check the market consistency of the intrinsic value derived from our DCF model. The definition of TPRO's peer group was primarily informed by the Company's underlying value drivers (see *Annex 8* for comparables selection). Consequently, the universe of pure-play probe card suppliers was not considered fully representative, given the pronounced divergence in business models.

The peer set was therefore extended to include selected semiconductor manufacturing equipment companies and precision component suppliers, which exhibit greater comparability to TPRO in terms of the mission-critical role of their products within leading foundries and IDMs' production processes, the elevated and sustained R&D intensity underpinning technological differentiation, the direct exposure to secular growth in semiconductor complexity driven by AI and advanced computing, and structurally high returns on capital employed.

Within the selected peer group, the OLS regression analysis highlights a weak association between EV/EBITDA and EBITDA margin FY25E, EBITDA margin 2026E and EBITDA CAGR FY25-27E, with none of the relationships exhibiting meaningful explanatory power (R^2 consistently below 20.0%). Conversely, the analysis indicates that equity valuations are predominantly driven by companies' ability to generate returns on capital employed, as evidenced by the **strong relationship between EV/CE and ROCE (R^2 of 80%)** (*Exhibit 35*).

The **1YF EV/CE multiple of 6.71x** implied by our analysis corresponds to a **target equity value of €15.83 per share**, closely aligned with the current market price. As an additional robustness check, we applied the same EV/CE-ROCE framework to FY25 fundamentals. Under this scenario, the **1YF EV/CE multiple of 5.48x** translates into an **equity value of €12.10 per share**, broadly in line with TPRO's observed market price of €12.20 at year-end 2025.

ESG grade attribution – Exhibit 36

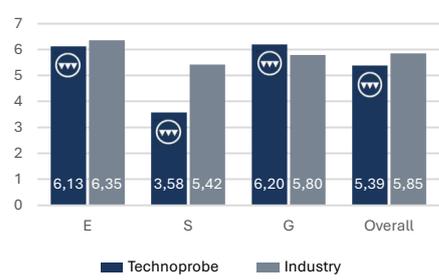
Combined ESG Score [Min-Max]	Grade
[9.17 - 10.0]	AAA
[8.34 - 9.16]	AA
[7.51 - 8.33]	A
[6.67 - 7.50]	BBB
[5.84 - 6.66]	BB
[5.01 - 5.83]	B
[4.17 - 5.00]	CCC
[3.34 - 4.16]	CC
[2.51 - 3.33]	C
[1.67 - 2.50]	DDD
[0.83 - 1.66]	DD
[0.0 - 0.82]	D



Source: LSEG

ESG Score Comparison – Exhibit 37

Overall: E weight 30%, S weight 30%, G weight 40%



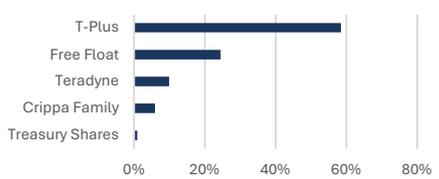
Source: Team Elaboration

Female Employees – Exhibit 38



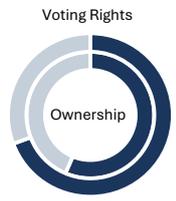
Source: Company Data, Team Assessment

Shareholders' structure – Exhibit 39



Source: Company Data, Team Estimates

Family Owned Business – Exhibit 40



Source: Company Data, Team Estimates

Risk matrix – Exhibit 41

IMPACT	LIKELIHOOD			
	Unlikely	Possible	Likely	Almost Certain
Disruptive	1., 14.	4., 12.	17.	
High	2., 10.	6., 9.	5.	
Moderate		11.	15.	3., 8., 13.
Marginal				

Source: Team Elaboration

Environmental, Social & Governance (ESG)

TPRO has only recently moved toward a more structured and formalized approach to Environmental, Social, and Governance (ESG) topics, reflecting the growing expectations of capital markets and institutional investors.

The Company began ESG reporting on a voluntary basis, with initial impact assessments in 2019 and the publication of Sustainability Reports from 2021 in line with **GRI Standards**, an internationally recognized framework for sustainability reporting developed by the Global Reporting Initiative. Since then, TPRO has progressively strengthened its ESG framework, including adherence to the Responsible Business Alliance (RBA) Code of Conduct and the publication of Non-Financial Statements for 2022 and 2023, signalling greater integration of sustainability into governance and Board-level oversight.

In 2024, this evolution advanced further with the transition to an Integrated Annual Report and the first Sustainability Statement prepared in accordance with the CSRD and ESRS. While these developments represent a meaningful step forward in disclosure quality and regulatory alignment, **TPRO's ESG profile remains transitional**. Transparency and formalization are improving, but full integration of ESG considerations into long-term strategy, capital allocation, and target-setting remains ongoing, particularly versus best-in-class global and European peers (*Exhibit 37, Annex 9*).

ENVIRONMENTAL	Score: B	Weight: 30%
----------------------	-----------------	--------------------

TPRO's environmental performance is characterized by **solid results in terms of emissions and resource consumption**, offset by limited efforts with respect to strategic ambition and regulatory alignment. Environmental disclosures now systematically cover **Scope 1, 2, and 3 greenhouse gas emissions**, with carbon intensity (Scope 1+2) of **56.1 tCO₂e per €m of revenue**, positioning the Company better than the direct peer-group average (68.0 tCO₂e/€m) (see *Annex 9*), though still above best-in-class performers such as FormFactor (29.9 tCO₂e/€m). A similar pattern emerges for water intensity, which stands at **333 m³ per €m of revenue**, significantly below the peer average (706 m³/€m), yet not at the efficiency frontier represented by leading peers. Energy efficiency represents one of the most tangible strengths within the environmental pillar. With an **energy intensity of 92.7 MWh per €m of revenue**, TPRO outperforms the industry average (158.1 MWh/€m); however the Company displays a very limited renewable energy mix compared to the European peer benchmark, remaining materially below sector averages.

On the other hand, TPRO shows weaker outcomes on regulatory and strategic indicators. In particular, the Company reports **no EU Taxonomy-aligned revenues**. Furthermore, while TPRO holds **ISO 14001 certification** and demonstrates improving transparency, the **absence of publicly disclosed, time-bound emission reduction targets** aligned with Science-Based Targets (SBTi) suggests that environmental management remains predominantly compliance-driven rather than strategically transformative.

SOCIAL	Score: C	Weight: 30%
---------------	-----------------	--------------------

TPRO's social profile presents a mixed but **clearly identifiable risk-opportunity balance**. Despite weaker performance in human capital development metrics, workforce composition represents a relative strength. **Training activity** averages 24.5 hours per FTE, below the European peer benchmark of 32.0 hours. Moreover, a **gender pay gap** of 29% compares unfavourably with both industry and European best practices. Conversely, women account for 34.1% of total employees – well above the peer average of 29.4% (*Exhibit 38*) – within a young, dynamic environment characterized by an average age of 34. Lastly, **R&D intensity** stands at 9.7% of revenues, materially below the peer average of 13.1%. While this indicator could imply R&D efficiency, it may also point to limited structural space for creativity and innovation.

From a qualitative perspective, TPRO has established **formal supply chain safeguards**, including a Supplier Code of Conduct and ESG screening procedures, alongside a consistent history of community engagement. While these elements align the Company with global minimum standards, **the Social pillar remains the least mature dimension of TPRO's ESG profile**, with clear room for improvement in training depth, pay equity, and the development of people-related KPIs comparable to leading multinational peers.

GOVERNANCE	Score: B	Weight: 40%
-------------------	-----------------	--------------------

TPRO's governance reflects a gradual shift from a **founder-led, family-centric model** toward a more institutional and multinational structure, though the process remains incomplete. The Crippa family maintains strong control through the proprietary holding T-Plus, which holds **56.4% of equity and 69.3% of voting rights** (*Exhibits 39–40*). This control is reinforced by a loyalty voting mechanism under which shares held continuously for **24 months acquire double voting rights**, strengthening long-term shareholder retention and amplifying voting power. Key roles remain concentrated within the family: Cristiano Crippa as Chairman, his brother Roberto Crippa as Vice Chairman, and their cousin Stefano Felici as CEO, centralizing strategic, financial, and capital allocation decisions.

Formal governance safeguards include a 10-member Board with **5 independent directors**, one director elected from the minority list, a Lead Independent Director, and dedicated committees (Control and Risk, Related Parties, Nomination and Remuneration). These mechanisms are aligned with the Italian Codice di Corporate Governance and act as counterbalancing measures to concentrated ownership. However, their effectiveness is partly constrained by the family's dominant role, which may limit diversity of viewpoints and Board-level debate.

The Euronext Milan listing (2023) introduced higher compliance and transparency standards and the presence of a limited number of strategic shareholders. However, the **low free float of 23%** remains a negative factor, as it may constrain liquidity and reduce overall market attractiveness. From an incentive-alignment perspective, the remuneration framework combines fixed pay with variable compensation linked to short term operational targets (EBITDA and revenues), complemented by Restricted Share Plans for executive directors and key management, supporting medium- to long-term value creation and retention. The adoption of ESG-linked remuneration together with SASB and TCFD frameworks further supports alignment between management and investor interests.

Investment Risks

This section identifies the **primary risks to our investment case** and evaluates how their evolution could impact our HOLD recommendation (*Exhibit 41*). The summary table on the following page provides our assessment of their potential impact on the DCF valuation.

Our analysis evaluates internal business risks, external market dynamics and competitive positioning within the broader macroeconomic landscape. While visibility remains relatively clear for the short term (2026), several threats emerge starting from 2027: (i) **AI CapEx cycle**: A potential downturn in 2027-2028; (ii) **HBM market entry**: Dependency on the adoption rate of proprietary Vertical MEMS technology; (iii) **Capacity expansion**: Execution risks associated with doubling production capacity by 2028; (iv) **Competitive pressures**: Intensifying rivalry in the low-end segment, which could erode TPRO's market share. Furthermore, Corporate Governance remains a key risk factor, specifically regarding high ownership concentration and a potential lack of managerial depth. Conversely, TPRO maintains significant upside potential in the long term from the Silicon Photonics (SiPh) market, conservatively reflected in our DCF.

TP Sensitivity Analysis 1 – Exhibit 43

		ΔRevenue Growth 27-30					
		-5%	-4%	-3%	-2%	-1%	0%
EBITDam 27-30	TP	12.85 €	13.28 €	13.71 €	14.16 €	14.62 €	15.09 €
	-6%	12.94 €	13.36 €	13.80 €	14.25 €	14.71 €	15.19 €
	-4%	13.02 €	13.45 €	13.89 €	14.35 €	14.81 €	15.28 €
	-2%	13.11 €	13.54 €	13.99 €	14.44 €	14.90 €	15.38 €
	0%	13.11 €	13.54 €	13.99 €	14.44 €	14.90 €	15.38 €

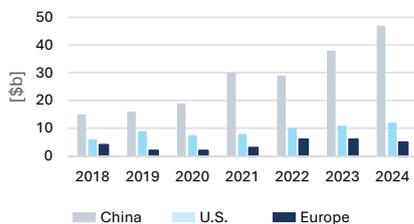
Source: Team Elaboration

TP Sensitivity Analysis 2 – Exhibit 44

		WACC				
		9.71%	9.46%	9.21%	8.96%	9.71%
Growth Rate	TP	13.24 €	13.85 €	14.52 €	15.25 €	16.05 €
	3.56%	13.57 €	14.22 €	14.93 €	15.71 €	16.58 €
	3.78%	13.93 €	14.62 €	15.38 €	16.22 €	17.14 €
	4.00%	14.32 €	15.06 €	15.87 €	16.77 €	17.77 €
	4.22%	14.74 €	15.53 €	16.40 €	17.37 €	18.46 €
	4.44%	14.74 €	15.53 €	16.40 €	17.37 €	18.46 €

Source: Team Elaboration

Semiconductor Spending by Region – Exhibit 45



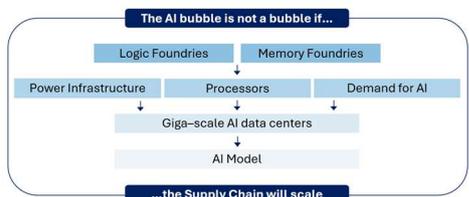
Source: Market Data

Impact Analysis – Exhibit 46

Risk	1st Impact	2nd Impact
1.	Revenue CAGR 2027-2030: -4%	EBITDam 2027-2030: -4%
2.	Revenue CAGR 2027-2030: -3%	EBITDam 2027-2030: -2%
3.	Revenue CAGR 2027-2030: -1%	EBITDam 2027-2030: 0%
4.a	Market Share HBM 2028-2035: +5%	EBITDam 2028-2035: +2%
4.b	Market Share HBM 2028-2035: -5%	EBITDam 2028-2035: -2%
5.	HBM Revenue CAGR 2028-2035: -3%	EBITDam 2028-2035: -2%
6.	Terminal Growth Rate: -0.44%	-
7.	Revenue CAGR SiPh 2028-2035: +15%	EBITDam 2028-2035: +2%
8.	NWC/Revenues: +32%	EBITDam 2026-2035: -1%
9.	Terminal Growth Rate: -0.44%	-
10.	Revenue CAGR 2027-2030: -3%	EBITDam 2027-2030: -2%
11.	-	EBITDam 2026-2035: -1%
12.	Terminal Growth Rate: -0.22%	WACC: +0.25%
13.	NWC/Revenues: +31%	EBITDam 2026-2035: -0.5%
14.	Revenue CAGR 2027-2030: -5%	EBITDam 2027-2030: -4%
15.	Revenue CAGR 2027-2030: -1%	-
16.	Directly on TP + 25%	-
17.a	Revenue CAGR 2027-2030: -4%	EBITDam 2027-2030: -4%
17.b	Revenue CAGR 2027-2030: -3%	EBITDam 2027-2030: -2%

Source: Team Elaboration

AI Data Center Supply Chain – Exhibit 46



Source: Team Elaboration

Gains (losses) due to Forex – Exhibit 47



Source: Team Elaboration

MARKET RISK

AI & Data Center	Risk Description: While the current expansion in AI data centers drives unprecedented demand for high-end probe cards, the sustainability of this CapEx cycle through 2027-2030 is not assured. Should AI software monetization fail to justify hyperscaler infrastructure investments at scale, the market risks entering a "digestion phase" characterized by sharp contraction in chip volumes. In this scenario, capacity expansion by TPRO would translate into acute underutilization, coupled with severe margin compression amplified by the Group's fixed cost base.
Likelihood	Impact
🌑	€13.36 /sh
Mitigation Strategies & Assessment: While largely exogenous, the risk is mitigated by TPRO's strong balance sheet. Its ~€600M net cash position provides roughly three years of operational runway, supporting continued R&D and strategic flexibility.	
Consumer, Edge AI	Risk Description: Consumer segment growth is primarily driven by Edge AI adoption. While the shift toward AI-enabled hardware increases test complexity and supports higher probe card ASPs, a failure to trigger mass device replacement cycles exposes TPRO to a "complexity trap": elevated R&D and manufacturing costs for sophisticated test solutions without sufficient economies of scale.
Likelihood	Impact
🌑	€13.89 /sh
Mitigation Strategies & Assessment: TPRO is reducing exposure to the Consumer, which represented ~50% of FY24 Revenues, in line with its 2026 strategic pivot toward AI and data centers. Consumer revenue is expected to decline to ~35% of total sales.	
Low-end Probe Card	Risk Description: Low-end probe card markets face intensifying price-based competition from lower-cost competitors where technological differentiation is minimal and products are increasingly commoditized. As customers prioritize cost optimization, TPRO's premium technology advantages provide limited pricing power in these segments.
Likelihood	Impact
🌑	€14.90 /sh
Mitigation Strategies & Assessment: TPRO is de-emphasizing these segments in favour of higher-margin, technologically advanced segments, reducing the impact of pricing pressure in commoditized markets.	
HBM Market Entry	Risk Description: HBM4E and HBM5 may not immediately require advanced testing solutions such as vertical MEMS, particularly if HBM stacks are not directly integrated onto the logic chip (e.g., in the HBM5 architecture). This could delay Technoprobe's penetration into the HBM testing market, giving competitors additional time to strengthen their offerings. As a result, Technoprobe may fail to fully capture potential gains in the HBM segment by 2028, with possible long-term implications.
Likelihood	Impact
🌑	€16.56 /sh €14.24 /sh
Mitigation Strategies & Assessment: Testing needs are shaped by foundry technology, but rising HBM complexity and advanced packaging are driving demand for more sophisticated testing solutions.	
HBM Cyclicity	Risk Description: The memory industry is structurally highly cyclical, characterized by sharp demand upswings followed by abrupt volume contractions driven by customer overstocking and inventory corrections. This cyclicity may result in periods of weaker demand for HBM-related testing solutions, negatively impacting volumes and revenue visibility.
Likelihood	Impact
🌑	€14.51 /sh
Mitigation Strategies & Assessment: Cyclicity is inherent to the memory sector, and HBM dynamics are largely predictable. In 2023, TPRO experienced the impact of this cyclical environment, which is exogenous and beyond the company's control.	
Chinese Competition	Risk Description: Chinese state-backed competitors are accelerating market penetration via subsidized financing, threatening TPRO's market share. Foundries in Taiwan and Korea may adopt Chinese secondary sources for cost optimization; furthermore, as domestic Chinese foundries strengthen, local probe card companies could lock TPRO out of the China Total Addressable Market.
Likelihood	Impact
🌑	€14.52 /sh
Mitigation Strategies & Assessment: TPRO's strategic pivot toward non-commoditized segments concentrates exposure on differentiated products beyond easy replication.	
SiPh & RF Expansion	Risk Description: The SiPh and RF testing markets are accelerating (CAGRs of 27.2% and 14.5% respectively) driven by hyperscaler adoption of 1.6T optical interconnects and the 6G rollout. TPRO's MEMS architecture is uniquely positioned to handle the extreme complexity of integrated waveguides and high-frequency matching networks, where legacy solutions fail.
Likelihood	Impact
🌑	€16.91 /sh
Mitigation Strategies & Assessment: TPRO maintains a critical first-mover advantage as competitors struggle with MEMS-SiPh integration. While NVIDIA (Mellanox) previously qualified FormFactor for early-stage applications, industry signals indicate a shift toward TPRO's advanced solution, potentially unlocking disproportionate revenue upside.	
Client Concentration	Risk Description: High customer concentration grants Tier-1 customers significant bargaining power, exposing TPRO to persistent margin pressure. Dependency extends Days Sales Outstanding (around 63 days) and last-minute ordering increases inventory carry costs, adversely affecting net working capital efficiency.
Likelihood	Impact
🌑	€14.90 /sh
Mitigation Strategies & Assessment: The probe card supplier base is highly concentrated, and major foundries have limited alternatives due to high switching costs and qualification timelines. Once locked into TPRO's architecture, this mutual dependency effectively constrains foundries' bargaining power.	

BUSINESS RISK

Innovation & Tech.	Risk Description: The rapid expansion of the semiconductor industry and the growing demand for increasingly advanced technologies are driving intensified R&D efforts by competitors aimed at closing the technological gap with TPRO or developing alternative testing solutions. This could weaken the company's competitive positioning over time.
Likelihood	Impact
🌑	€14.52 /sh
Mitigation Strategies & Assessment: TPRO benefits from a structural competitive advantage through its leadership in Vertical MEMS. Consistently advancing its technology via R&D and product innovation, the company is well-positioned to maintain this edge.	
Capacity Expansion	Risk Description: TPRO's plan to double production capacity by 2027 entails significant execution risk. The aggressive expansion timeline is exposed to several potential bottlenecks, including: excavation and construction constraints, delays in clean-room certifications and misalignment of management systems between existing sites and the new facility. Any such friction could slow fixed-cost absorption, turning this CAPEX deployment into a near-term headwind for operating margins and free cash flow generation.
Likelihood	Impact
🌑	€13.89 /sh
Mitigation Strategies & Assessment: With the construction of a new integrated facility, the Group is moving toward a lean operating model. Additionally, space has already been allocated within existing plants to support a 15–20% production increase.	
Talent, Key Figures	Risk Description: The structural shortage of specialized MEMS and semiconductor engineers in Europe limits TPRO's operational scalability. Competition for STEM talent from adjacent industries, coupled with ongoing brain drain to US and Asian semiconductor hubs, may increase turnover among key technical staff. Insufficiently competitive compensation and incentive structures could raise OPEX through higher retention costs and slow R&D, undermining the company's competitive positioning.
Likelihood	Impact
🌑	€14.97 /sh
Mitigation Strategies & Assessment: TPRO benefits from an attractive work environment, with ~16% employee turnover and a young workforce (average age ~35). Ongoing and planned share buybacks support equity-based compensation, strengthening retention.	
Governance	Risk Description: High ownership concentration (Crippa family controls ~67.9%) creates governance constraints. Leadership possesses elite technical backgrounds but exhibits deficit in formal managerial and financial depth. This risk exposes the Group to suboptimal capital allocation and ineffective financial risk management.
Likelihood	Impact
🌑	€14.22 /sh
Mitigation Strategies & Assessment: TPRO is enhancing its governance toward a more institutional structure, including the appointment of independent board members and strategic partnerships with Teradyne and Advantest. Despite recent buybacks, the founding family has also expressed willingness to partially dilute its stake to attract experienced capital and operational expertise.	
Supplier Exposure	Risk Description: TPRO remains exposed to supply and price risks for ceramic substrates, advanced chemical materials, and precious metals. Supply chain disruptions could force production slowdowns, while unfavourable supplier dynamics, given TPRO's unsubstantial bargaining power, could compress Days Payable Outstanding (DPO).
Likelihood	Impact
🌑	€ 15.13/sh
Mitigation Strategies & Assessment: TPRO's vertical integration reduces exposure to third-party supply and lead-time volatility, while its MEMS-based architecture lowers precious metal usage, limiting price risk.	

MACROECONOMIC RISK

Hub Localisation	Risk Description: TPRO's financial performance is highly exposed to the Taiwanese semiconductor ecosystem, creating a material geographic concentration risk. Taiwan remains the primary hub for advanced-node (N3, N2) and AI chipset production; any geopolitical escalation or disruption in the Taiwan Strait could halt wafer starts, leading to a sharp decline in demand for high-end MEMS probe cards. TPRO's high operating leverage would amplify the resulting financial impact.
Likelihood	Impact
🌑	€12.94 /sh
Mitigation Strategies & Assessment: TSMC's capacity expansion in the US and Germany should gradually mitigate concentration risk over the medium term. However, exposure is expected to remain elevated through 2026–2027, as advanced-node production is likely to stay predominantly Taiwan-based.	
Export Control	Risk Description: Geopolitical trade policies between the U.S. and China pose risks to the semiconductor sector. Recent export restrictions on advanced chips to China have reduced the addressable market for fabs and foundries, impacting TPRO's end markets.
Likelihood	Impact
🌑	€14.90 /sh
Mitigation Strategies & Assessment: While TPRO is exposed to these dynamics, semiconductor demand in Western and non-China Asian markets remains sufficiently large to offset the impact in the near term. In addition, TPRO is not affected by U.S. tariffs, as the semiconductor – and specifically the probe card – segment is exempt from measures introduced under the Trump administration.	

FINANCIAL RISK

Industrial Takeover	Risk Description: There is a limited risk that TPRO could become an acquisition target for larger semiconductor players seeking to strengthen their testing capabilities and gain a broader competitive advantage.
Likelihood	Impact
🌑	€19.23 /sh
Mitigation Strategies & Assessment: Management remains open to strategic industrial partnerships aligning with long-term value creation. To date, no formal proposals have been received.	
ForEx (EUR/USD)	Risk Description: TPRO has a structural currency mismatch, with ~90% of revenues denominated in USD and ~80% of operating costs in EUR. This unhedged exposure increases earnings volatility, introducing a non-operational risk factor that may drive deviations from guidance.
Likelihood	Impact
🌑	€16.93 /sh €13.94 /sh
Mitigation Strategies & Assessment: TPRO does not currently employ a material FX hedging program, leaving earnings fully exposed to currency movements, with asymmetric downside in the event of EUR appreciation.	

The End-to-End Microchip Value Chain 11

Product Description 12

Future Trends 13

Experts Verdict & M&A Track Record 14

Timeline of Growth and Moat Consolidation (1996-2025E) 15

Competitive Financial Positioning 16

Valuation 17

Valuation 18

ESG 19

Corporate Governance Relevant Risks 20

1. The End-to-End Microchip Value Chain

Phase / Stage	Infrastructure & Components	Visual Reference	Functional Description & Strategic Impact	Key Players
Chip Design	EDA (Electronic Design Automation) / CAD (Computer-Aided Design) tools and IP (Intellectual Property) cores.		Engineers define the micro-architecture, logic, and physical layout of the IC (Integrated Circuit) to create the digital blueprint	Fabless Companies NVIDIA, AMD, Qualcomm, Apple
Probe Card Design	Specialized engineering software and co-design frameworks.		Parallel to IC design, engineers develop a custom electromechanical interface tailored to mirror the specific pad layout of the new chip	Probe Card Makers TECHNOPROBE, FORMFACTOR™
Wafer Fabrication	Fabs (Fabrication Plants), photolithography machines (EUV/DUV - Extreme/Deep Ultraviolet), and raw silicon.		Raw silicon is processed into wafers, where nanometer-scale transistor structures are chemically and physically etched onto the substrate	Foundries SAMSUNG, GlobalFoundries, intel, UMC, TSMC
Wafer Test / Sort (TPRO's Core)	The equipment ATE (Automated Test Equipment) and Wafer Prober.		During wafer testing, a high-performance mainframe computer within the Automatic Test Equipment (ATE) generates and analyzes electrical signals to verify the circuit's logic and functionality. This system controls the test sequence and supports the EDS (Electrical Die Sorting) process used to identify defective dies before packaging.	ATE Providers TERADYNE, ADVANTEST, Cohu, ficonTEC
	The Interface Probe Card manufactured with TPEG™ (Technoprobe Proprietary Etching and Galvanic) Vertical MEMS technology.		The connection between the ATE and the wafer is provided by the probe card , a highly precise interface designed to make temporary electrical contact with the microscopic pads of each die. It ensures accurate signal transmission and reliable measurements at the wafer level	Probe Card Makers TECHNOPROBE, FORMFACTOR™
	The Target The Processed Silicon Wafer		The test is performed directly on the physical silicon wafer , which contains multiple individual chip dies. Each die is electrically verified during EDS (Electrical Die Sorting), allowing faulty units to be identified and excluded before the wafer is diced and the good dies are packaged	Foundries SAMSUNG, GlobalFoundries, intel, UMC, TSMC
Assembly & Packaging	Dicing saws, substrates, and OSAT (Outsourced Semiconductor Assembly and Test) plants.		The wafer is diced into individual chips; functional dies are then encapsulated in protective housings with external connections, a process typically performed by OSATs	OSATs ASE, Amkor Technology, JCET
Final Test (TPRO's new entry)	The equipment Test Controller (ATE) and Handlers		During the final test, automated test systems manage the handling of packaged devices and generate the electrical test vectors required to verify performance and functionality after assembly	ATE Providers TERADYNE, ADVANTEST, Cohu
	The interface DIB (Device Interface Board) and Test Sockets		The electrical connection between the tester and the device is provided by the Device Interface Board (DIB) – integrated by Technoprobe through the DIS acquisition – which routes signals accurately from the test system to the package.	DIB Card Makers DIS TECH, GMP, LEENO
	The target Device Under Test (DUT): The Packaged Chip		The Device Under Test (DUT) is the fully assembled chip. It undergoes comprehensive electrical and thermal stress tests to ensure it was not damaged during packaging and meets all final reliability and performance requirements before shipment	OSATs ASE, Amkor Technology, JCET
System Integration	SMT (Surface Mount Technology) and PCBs (Printed Circuit Boards)		Validated microchips are mounted onto PCBs and integrated into final electronic products, such as servers or smartphones, a step typically carried out by OEMs (Original Equipment Manufacturers)	OEMs FOXCONN, DELL, hp, TESLA

Source: Team Elaboration

2. Product Description

I. Product Portfolio

Op. Segment	Products Category	Product Type	Function/role	Order winners	Level of innovation*	IP positioning**	Main Brand	
Wafer-level test	Probe Cards	TPEG™ Vertical MEMS	Electrical testing of high-end semiconductor dies on wafer (wafer-sort / wafer probe)	Extremely high probe density, supports advanced nodes (5 nm, 3 nm+), high precision, reliability, customer-specific	H	Requires MEMS micro-fabrication to hit very fine pitches	1	
		Vertical (non-MEMS)	Wafer-level electrical test, for simpler or legacy wafers	Lower cost than MEMS, reliable, fast turnaround	M	Mature design with limited innovation.	2	
		Cantilever	Wafer-level test for legacy or specialized wafers	Flexibility for pad layouts, cost-effective for less advanced processes	L	Legacy tech; innovation mostly due cost/reliability	3	
Final test Solution	Device Interface Solutions	Device Interface Board (DIB) / Final Test Board	Electrical interface between packaged devices and automated test equipment	Wide package support, reliability, interface quality, compatibility with ATE, vertical integration	M	Complex PCBs but well-established engineering	2	
	Test Sockets	Final Test Motherboard	Enable functional testing of packaged semiconductors after assembly	Mechanical reliability, high contact durability, flexible package support, ease of integration with ATE	M	Proven mechanical tech with small refinements	2	

*Level of innovation: H-high; M-medium; L-low

**TPRO positioning: 1-leader; 2-follower with relevant position; 3-follower

Source: Team Estimates

II. Flagship Product: the Probe Card

Component	Visual Reference	In House	Description
Stiffner		✓	Provides the structural integrity and planarity required for reliable wafer contact. It interfaces with the probe, manages contact forces, and compensates for thermal expansion to ensure repeatable performance across multiple test cycles.
PCB		✗	Printed Circuit Boards serve as the signal routing and power distribution backbone , connecting the tester to the probes. Advanced PCBs use low-loss materials to preserve signal integrity in high-frequency applications.
Interconnection		✓	Electrically links the PCB to the probe elements, enabling stable high-speed and high-current signal transmission . Its design ensures reliability under thermal and mechanical stress during repeated probing.
Probe head	Ceramic plates	✓	Provide mechanical rigidity, thermal stability, and electrical insulation , ensuring precise probe alignment and consistent performance.
	Contact probes	✓	Needles that form the electrical interface with the wafer, and are designed for fine pitch, low contact resistance, high durability, and minimal pad damage , directly impacting test yield and throughput .

Source: Company Data, Team Elaboration, Team Visual Representations

3. Future Trends – Technology Overview and TPRO Strategic Positioning

I. Chiplet Revolution

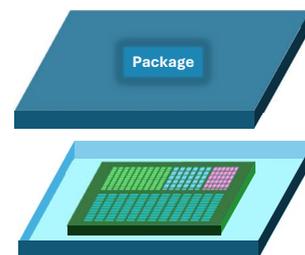
The semiconductor industry has reached a **reticle size limit** where traditional monolithic scaling is no longer economically or physically viable. This **architectural pivot to chiplets** transforms semiconductor testing from a back-end commodity into a **mission-critical 'yield insurance' policy**, placing TPRO at the center of the Advanced Packaging value chain.

Sistem On Chip (SoC)	Chiplet
<p>Legacy Monolithic SoC Historically, all components were integrated on one die. This "all-or-nothing" approach concentrates risk: a single defect scraps the entire expensive unit. Testing here is a final gatekeeper with limited ability to recover high manufacturing losses.</p>	<p>Disaggregated Chiplet Architecture Modern designs use modular chiplets. This requires a shift-left testing strategy: TPRO verifies each chiplet as a Known Good Die (KGD) before assembly. This acts as a volume multiplier for TPRO, as precision testing becomes mandatory to avoid scrapping expensive assemblies.</p>

ADVANCED PACKAGING

Chiplet-based architectures rely on advanced packaging technologies, such as **2.5D integration and 3D stacking**, to combine multiple dies into a single system. Once these dies are interconnected, a defect in any individual component can jeopardize the entire package, making post-assembly failure extremely costly. To mitigate this risk, testing is moved earlier in the manufacturing flow, requiring each die to be certified as a KGD prior to assembly. This shift elevates wafer-level testing from a supporting step to a critical determinant of yield and reliability, positioning high-performance probe cards as a key enabler of advanced packaging.

Legacy Packaging (Standard Interconnects)	Advanced Packaging (High-Density Integration)
Historically, semiconductor packaging mainly provided physical protection and electrical connection between the die and the PCB. Techniques such as wire bonding and standard flip-chip used relatively large interconnects, typically above 100µm pitch. In this model, the package had minimal impact on performance and was treated as a back-end commodity, with connectivity verification requiring limited precision.	Advanced Packaging marks a shift in which the package becomes a performance-critical part of the architecture. Technologies such as 2.5D interposers and 3D stacking integrate multiple dies into a single unit using micro-bumps and TSVs, pushing interconnect pitches below 40µm. The result is a dense, high-bandwidth network of connections where packaging directly affects performance, power efficiency, and reliability.

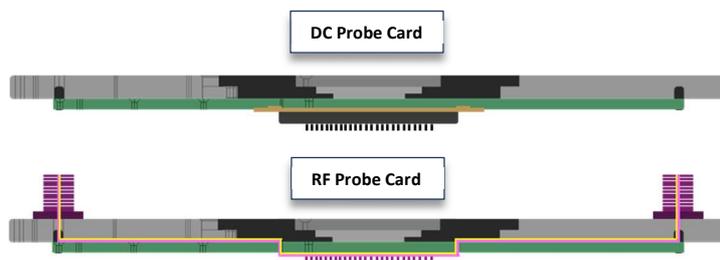


Source: Team Elaboration, Team Visual Representations

II. Hyper Scaling of AI Interfaces

The Engineering Challenge: Overcoming the Interconnect Bottleneck

As AI interfaces transition to 224 Gbps data rate (speed of information transfer), the physical path between the tester and the silicon die becomes the primary source of signal degradation. Traditional **DC (Direct Current) probe cards**, designed for low-frequency parametric testing, are insufficient at these data rates, where tiny imperfections in the signal path act as a brick wall for data. **RF (Radio Frequency) probe cards**, engineered for high-speed signaling, address this challenge by minimizing signal path length and maintaining shielding continuity from the tester interface directly to the probe tip. By focusing on signal control, TPRO preserves high-frequency integrity for AI workloads, preventing false failures that would otherwise undermine manufacturing efficiency in the "Terabit Era."



Setting the Technology Benchmark

Feature	General RF Market	FormFactor (Pyramid RF)	TPRO (UltraPhantom)	Strategic Implication
Max Frequency	20 – 40 GHz	~81 GHz	Up to 150 GHz	TPRO covers 2x the required AI bandwidth.
Signal Integrity	Basic Shielding	High-End Air-Coplanar	Advanced Coaxial MEMS	Lower noise floor for 224 Gbps signaling.
Pitch Capability	>150 μm	~125 μm	100 μm (Fine Pitch)	Enables testing of denser AI interconnects.
Application Focus	4G/5G, Consumer IoT	Advanced 5G, Networking	Gen-AI & Terabit Data Centers	TPRO is aligned with the highest-growth vertical.
R&D Initiative	Maintenance CAPEX	Incremental	'Terabit Era' (€12.5M)	Sustained leadership in next-gen standards.

Source: Company Data, Team Elaboration, Team Visual Representations

III. HBM – High Bandwidth Memory

The rapid scaling of Generative AI has shifted the semiconductor value chain's focus toward **High Bandwidth Memory (HBM)**, currently the primary bottleneck for AI accelerator performance. While the HBM testing market has historically been dominated by incumbents utilizing legacy micro-cantilever probe cards, the industry transition to **HBM3E and HBM4** architectures, characterized by 12 and 16-layer vertical stacks, presents a significant entry catalyst for TPRO. As technical requirements for pitch density and thermal management exceed the physical limits of cantilever technology, TPRO's proprietary technology may play a role in supporting manufacturer yield recovery

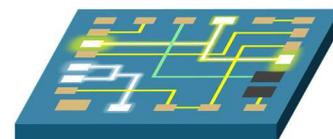
PROBLEM	SOLUTION		
<p>The Cost of Undetected Latent Defects As HBM density scales to 12–16 layers, manufacturers increasingly face the "Compounded Yield Wall." A single defective DRAM die can pass wafer-sort because legacy probe cards lack the signal integrity needed to fully stress high-speed interfaces. Once that die is permanently integrated into a 3D stack via TSVs (Through-Silicon Via) – along with 12 DRAM layers and a base logic die – the defect is no longer recoverable. A failure discovered after stacking forces the disposal of the entire high-value assembly, resulting in significant gross-margin loss and wasted CapEx on otherwise functional components.</p>	<p>Strategic Mitigation via Vertical MEMS Technoprobe's TPEG™ Vertical MEMS technology transforms the testing phase from a cost center into "Yield Insurance." By providing ultra-high-fidelity contact and superior planarity, TPRO enables Known Good Die (KGD) verification with near-100% accuracy before the stacking process begins. By isolating "red dies" at the wafer level, TPRO ensures that only verified components enter the assembly line. This eliminates post-stacking scrap, optimizes the manufacturer's Total Cost of Ownership (TCO), and provides the mechanical precision required for the sub-30μm pitches of the upcoming HBM4 cycle.</p>		
Incumbent Specifications	Description (Legacy Architecture)	Technoprobe Specifications	Description (Advanced MEMS)
Micro-Cantilever Technology	Utilizes horizontal needle architecture. The scrubbing motion required for contact risks damaging fragile HBM micro-bumps and TSVs.	TPEG™ Vertical MEMS	Proprietary vertical "plunge" contact. Eliminates lateral stress, preserving the structural integrity of high-density 16-layer stacks.
Pitch Scalability Limits	Mechanical constraints of cantilever needles make reaching sub-40μm pitches difficult, creating a bottleneck for next-gen HBM4.	Sub-30μm Lithography	Leverages advanced semiconductor-like lithography to achieve the ultra-fine pitches required for the 2048-bit HBM4 interface.
Thermal Drift Sensitivity	Prone to needle misalignment during high-temperature testing due to material expansion differences.	Active Thermal Stability	Uses proprietary low-CTE (Coefficient of Thermal Expansion) alloys that maintain nanometer precision from -55°C to +150°C.
Fragmented Supply Chain	Reliance on third-party manufacturers for substrates and components results in standard 12-16 week lead times.	Full Vertical Integration	In-house manufacturing of both MEMS probes and MLO substrates reduces development cycles by ~40% (Time-to-Market advantage).

Source: Team Elaboration, Team Visual Representations

IV. Silicon Photonics (SiPh)

Silicon photonics integrates optical components onto silicon chips, allowing light to be generated, guided, modulated, and detected alongside electronic circuits. By using existing semiconductor processes, it enables **high-speed, low-power interconnects** that surpass copper, offering scalable, cost-efficient solutions for data centers, high-performance computing, and sensing. By combining optics and electronics on a single platform, it supports faster, more energy-efficient information processing and communication.

Component	Function
Lasers (external or hybrid)	Generate the light. Since silicon struggles to emit light, materials like InP (Indium Phosphide) are added to the chip.
Waveguides	Channels that guide light across the chip (like wires for photons). Usually made of silicon with SiO ₂ cladding.
Modulators	Convert electrical signals into optical signals.
Photodetectors	Convert light back to electrical signals, often using germanium-on-silicon photodiodes .
Filters/Resonators	Control wavelength selection and routing.
Couplers/Gratings	Move light in and out of the chip, e.g., from fiber to chip.



Future Applications and Considerations

In the short term, silicon photonics is transforming **data centers** by enabling ultra-fast, energy-efficient interconnects that reduce latency and power consumption. Looking further ahead, it holds promise for **LIDAR systems**, where it could significantly reduce the size and cost of optical sensors used in autonomous vehicles, robotics, and advanced sensing. **Transceivers** that combine photonics and electronics are already paving the way for next-generation high-speed communication. However, photonics also faces fundamental **limitations**: optical components cannot be smaller than the wavelength of the light they carry (around 1 micrometer), whereas electronic components operate at the scale of just a few nanometers. This means silicon photonics alone cannot achieve the extreme integration densities of traditional electronics. As a result, the industry is moving toward **hybrid packaging solutions** that pair photonic chips with conventional electronic chiplets, leveraging the strengths of both technologies. This combined approach ensures that we get the **speed and energy efficiency of light** while retaining the **compact, highly integrated capabilities of electronics**.

Source: Team Elaboration, Team Visual Representations

4. Experts Verdict

INSIDER INTELLIGENCE: The View From Within

Interviewee Category	Citation Themes		
	Competitive Moat & Technological Edge	Growth Drivers: AI, HBM & Next-Gen Tech	Financial & Operational Risks
Board & Executive Management	"Listing wasn't just about capital; it was a challenge to institutionalize excellence and force ourselves to meet global standards that a family-run business might otherwise ignore."	"Our HBM roadmap is a calculated evolution, targeting at least a 10% market share within four years, supported by vertical MEMS superiority."	"The ' 90/80 mismatch ' – 90% USD revenues against 80% EUR costs – is a structural vulnerability. A weakening dollar can erode our EBITDA margin"
Operational Staff & R&D	"In an industry defined by intense turnover, Technoprobe is an island of stability. In a decade here, I've seen the technology transform, yet the faces remain . We don't just stay for the innovation; we stay because the culture breeds fulfillment."	"We are pushing the boundaries of density, aiming for 150,000-pin probe cards . We are moving toward a world where the 'package' disappears, and testing happens directly on the wafer."	"The 'bullwhip effect' is real. August and February are our battlegrounds where we must hit a peak capacity of 130 cards per week to satisfy the consumer electronics cycle."

ECOSYSTEM SYNERGY: Partners on the Frontline

Interviewee Category	Citation Themes	
	The Technology Partnership	The Market Dynamics
ATE Integration	"Technoprobe has transcended the role of a vendor to become an essential co-engineering partner . As high-performance AI chips scale toward thousands of watts , the probe card has evolved into a mission-critical hybrid: a high-density electrical conduit and an advanced thermal management system ."	"The market is a 'One-Stop-Shop' race. While we provide the brain (the tester), Technoprobe provides the nervous system (the probe card). One cannot scale without the other."
Supply Chain & Reliability	" The cost of failure is astronomical . A single defective pin can compromise a multi-thousand-dollar AI wafer. 'Dead on arrival' is not an option for our tier-1 clients."	" Local Asian competitors excel at fast-follower strategies , offering lower-cost replicas once designs stabilize, forcing Technoprobe to continuously innovate."

MARKET REALITY CHECK: Independent Industry Perspectives

Interviewee Category	Citation Themes	
	Competitive Benchmarking	Investment Narrative
The Competitor View	"Technoprobe's vertical integration is their greatest defense . By controlling the ceramic and the MEMS process, they maintain margins that fabless competitors simply cannot match."	"The battle for Memory (HBM) is the next great frontier. While we currently hold the monopoly, Technoprobe's entry into this segment is the single biggest threat to the status quo."
Experts View	"Technoprobe is currently a ' pure play ' on Nvidia's GPU dominance . They hold a near-monopoly on high-end logic testing, which justifies their premium valuation over traditional tech."	"At 80x earnings , the market is pricing in a flawless execution of the HBM strategy. The upside is clear, but the margin for error has never been thinner."

Source: Team Elaboration

5. M&A Track Record & Description

I. M&A History Phases and Strategic Rationale

Phase	Years	Strategic rationale	Key Acquisitions & Events
I. Core Moat Building and IP Consolidation	2019	Internalization of Micro-fabrication for Probe Needles: Technoprobe acquired proprietary technology (MICA FREEFORM™) and expertise for manufacturing complex micro-components. This step secured the internal capability to produce high-precision probe needles, reducing dependency on external IP and directly strengthening the core Vertical MEMS competence .	Microfabrica Inc. (Acquired 100% in May 2019 and production facility dismissed in 2025).
II. Vertical Integration and Final Test Enabler	2023 – Mid 2024	Control of AI Test Bottlenecks (PI/SI): TPRO strengthened its position by acquiring high-performance interconnect IP (Fusion Link via Harbor) and DIB design capabilities (via DIS Tech), addressing PI/SI bottlenecks in high-current AI/HPC testing. This reinforced its probe card moat and enabled expansion into the adjacent Final Test Solutions market.	Harbor Electronics (Acquisition of IP/assets, 2023) and DIS Tech (Acquired 100% in May 2024 from Teradyne).
III. Strategic Ecosystem Alignment and HBM Acceleration	Late 2024 – 2025	ATE Partnership and HBM Qualification: Integration of key Automated Test Equipment (ATE) leaders into TPRO's shareholder base to ensure technological alignment for next-generation platforms (HBM4/5). This strategic validation accelerates the HBM revenue opportunity and secures critical MLO substrate capacity in Taiwan to support the subsequent volume ramp-up.	Strategic Investments: Teradyne acquired a 10% stake in TPRO (May 2024), Advantest acquired a 2.5% stake (Jan 2025), and Yee Wei Inc. acquired minority interests in H1 2025 to support capacity consolidation.

Source: Team Elaboration

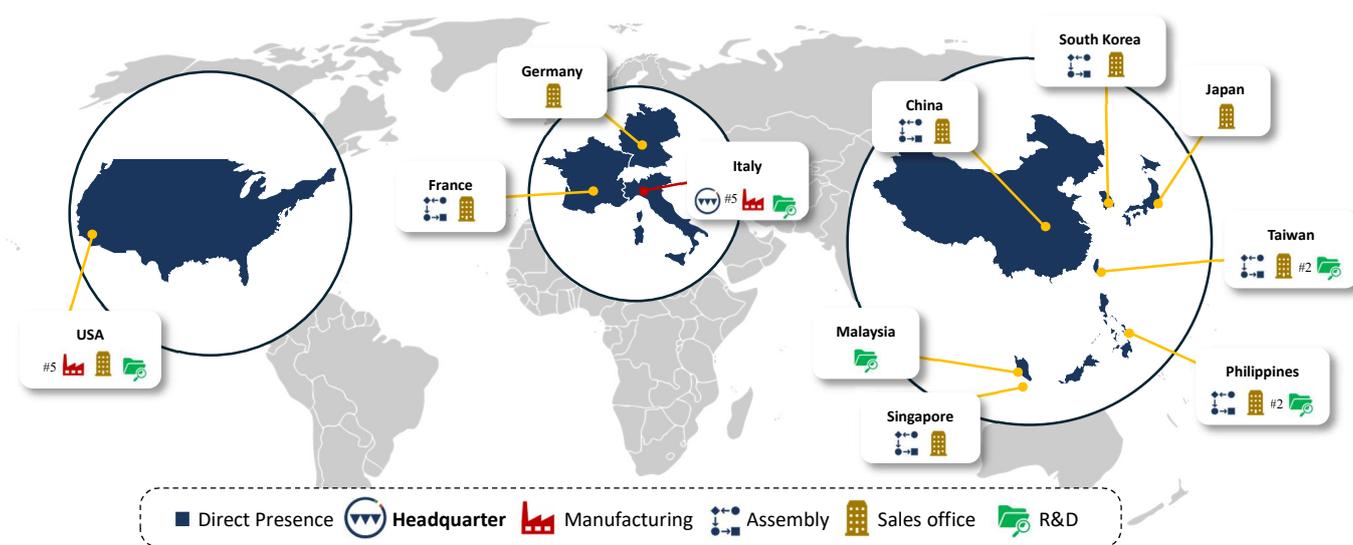
II. M&A Financial Overview and Key Metrics

Company	Stake Acquisition	Acquisition year	Target's country	Acquirer vehicle	Consideration [€m]	Consideration / Contributed Revenues	Goodwill* [€m]	Goodwill/Equity
Microfabrica Inc.	100%	2019	US	Technoprobe S.p.A.	33	N/A	10	4.0%
Yee Wei Inc.	85% (Initial) 100% (Final)	2022 2025	Taiwan	Technoprobe S.p.A.	10 20	N/A N/A	N/A N/A	- -
Harbor Electronics	100%	Aug 2023	US	Technoprobe S.p.A.	46	0.96	15	1.8%
MW Plasma Inc.	80%	Dec 2023	US	Yee Wei Inc.	Not Disclosed	Immaterial	Not Disclosed	-
DIS Tech	100%	May 2024	US / Asia	Technoprobe S.p.A.	82	0.9	20	1.6%
Innostar Service Inc.	9.37%	Jan 2025	Taiwan	Technoprobe S.p.A.	7	N/A	N/A	-

* Goodwill is the difference between the Consideration Paid and the Fair Value of Net Assets Acquired

Source: Team Elaboration

6. Timeline of Growth and Moat Consolidation (1996-2025E)



Year	Country	Company / Expansion	Strategic Rationale (Impact on TPRO)
1996	Italy	Technoprobe Foundation: Company founded in Cernusco Lombardone, Italy.	Core Business Foundation. Launched with a focused strategy on developing and manufacturing high-end probe card technology, under the leadership of founder Giuseppe Crippa.
2001	France	TP France: First international subsidiary established.	Initial European Presence. Began establishing local sales and support infrastructure outside Italy
2002	China	TP Singapore: First office opened in Asia.	First Asian Foothold. Established a presence in the APAC market for local production support.
2008	USA	TP America: US facility opened in California (Silicon Valley).	Outpost in Silicon Valley. Placed a technical base near major US fabless companies for co-design collaboration.
2010	Philippines	TP Philippines: Operations established in the Philippines.	Logistics and Assembly Expansion. Provided support for production and assembly activities in Southeast Asia.
2011	Italy	TP Italy Expansion: Expansion of the main Cernusco Lombardone production site.	Consolidation of Core Capacity. Increased Italian capacity for R&D and high-complexity manufacturing of the TPEG™ MEMS technology.
2015	South Korea	TP Korea: Subsidiary established in South Korea.	Proximity to Memory Market. Placed a local support center near major Korean Memory manufacturers.
2017	Italy	Grand Opening of new HQ and fab in Italy	Significant investment to solidify Italy as the central hub for R&D and high-complexity manufacturing, enabling global scale.
2019	USA	Acquires Microfabrica Inc.: Acquisition of the specialized micro-fabrication company.	IP Moat Building (Phase I). Internalized critical <i>additive</i> manufacturing IP (MICA FREEFORM™), essential for building advanced, high-precision Vertical MEMS probes.
2019	Taiwan	TP Taiwan: Subsidiary established (Technoprobe Taiwan Co Ltd).	Vertical Integration Precursor. Established local presence critical for later MLO substrate development and close proximity to TSMC.
2019	Japan	TP Japan: Subsidiary established (Technoprobe Japan KK).	Global Service Network Completion. Established a design and service center to serve the Japanese market.
2019	Germany	TP Germany: Subsidiary established (Technoprobe Germany GmbH).	Global Service Network Completion. Placed sales presence in Germany, important for the European Automotive sector.
2019	China	TP China: Subsidiary established (Technoprobe Suzhou Co Ltd).	Global Service Network Completion. Established direct commercial and support presence in the Chinese market.
2021	Italy	New fab and offices (Agrate, Osnago)	Expanded specialized MEMS and photolithographic capacity, supporting the continuous development of next-generation <i>probe cards</i> .
2022	Italy	Listed on Euronext Growth Milan Market	Access to Capital and Visibility. IPO completed (Feb 2022). Secured capital to fund aggressive expansion and R&D.
2022	Italy	New Design Center in Catania	R&D Talent Expansion. Established a new R&D and software design center in Southern Italy, investing in the engineering talent pool.
2022	Taiwan	Acquires 85% stake in Yee Wei Inc. (Acquired from Genius Pack AG).	Vertical Integration (MLO Substrates). Formalized control over critical Multi-Layer Organic (MLO) substrate technology for Power Integrity (PI).
2023	Italy	Transition to Euronext Milan Market	Enhanced Governance Standards. Transferred to the regulated market (May 2023), raising compliance standards for institutional investors.
2023	USA	Acquires Harbor Electronics: Acquired IP and assets related to high-performance interconnects.	Vertical Integration (Fusion Link). Internalized Fusion Link IP for advanced PCB design, critical for managing SI/PI in high-current AI testing.
2023	Italy	Acquires MW Plasma: Acquired MW Plasma Inc.	Technological Diversification. Technological diversification through a targeted acquisition focused on specialized industrial processes, specifically plasma-based technologies.
2024	USA	Acquires DIS Tech: Acquired the Device Interface Solutions (DIS) division from Teradyne. Teradyne concurrently acquires a 10% stake in TPRO.	Full Vertical Integration & ATE Partnership. Gained control over Device Interface Board (DIB) design competency, completing the test interface chain. The concurrent investment formalized strategic alignment with a major ATE leader.
2025	South Korea	Advantest Partnership: Advantest acquired a 2.5% stake in TPRO.	Ecosystem Alignment. Reinforcement of TPRO's indispensable role, accelerating co-development and qualification for next-generation test platforms, particularly for the HBM revenue ramp.
2025	Taiwan	Acquires Innostar Service Inc. (9.37% stake): Minority stake acquisition (for €6.6M) in a Taiwanese company.	Automation & Advanced Packaging. Gained a strategic stake to optimize MEMS production (via Automated Probe Insertion and AOI & Repair Lines) and accelerate integration into Advanced Packaging workflows, specifically for Copper Pillar and Mass Transfer.
2025	Taiwan	Yee Wei Inc. (100%): Completed acquisition of the remaining minority interests (H1 2025).	Full Control of Critical Substrates. Secured 100% control over MLO substrate design and production capacity (Yee Wei), completing the vertical integration strategy and technical control over highly complex components.

Source: Company Data, Team Elaboration

7. Competitive Financial Positioning

2024	Size & Growth		Margins			Investment Intensity			Balance Sheet Quality
[\$m]	Revenue	Revenue CAGR 19-24	Gross Margin	EBITDAm	EBITm	CapEx/Sales	CapEx/D&A	R&D/Revenue	Goodwill/Equity
Technoprobe	586	20.7%	41.1%	25.1%	12.3%	17.6%	166.4%	9.7%	3.7%
FormFactor, Inc	767	5.3%	41.7%	17.2%	11.8%	5.0%	96.2%	16.0%	21.0%
Japan Electronics Materials	163	2.3%	39.7%	-	19.2%	14.5%	303.8%	6.2%	-
Micronics Japan Co.	368	7.4%	48.8%	27.7%	22.6%	20.2%	395.0%	9.2%	-
MPI Corporation	308	10.8%	54.7%	32.0%	24.4%	2.1%	37.4%	11.0%	-
WinWay Technology	177	13.5%	43.7%	28.6%	23.6%	4.6%	109.9%	6.1%	-
Average Competitors	356	7.0%	45.7%	26.4%	20.3%	9.3%	188.4%	9.7%	21.0%

Source: FactSet, Team Elaboration

8. Valuation

WACC Computation

TPRO has a debt-free capital structure, and therefore its **WACC is computed solely based on the cost of equity**. No adjustments for the cost of debt making the WACC equivalent to the computed cost of equity, which is estimated at 9.21%.

COST OF EQUITY

Market Beta

TPRO's Market Beta was estimated by combining regression-based approaches with a peer-group analysis, in order to account for the structurally higher cyclicality of the semiconductor sector, which may not be fully reflected in broader equity market indices.

Fama–French Three-Factor Model

We applied the Fama–French three-factor model by estimating market (β_m), size (β_s), and value (β_v) factor loadings through a multivariate regression of TPRO's weekly returns (25 February 2022 -19 December 2025) against STOXX 600 excess returns and SMB and HML factor portfolios constructed from MSCI Europe indices. The regression results are affected by a high degree of collinearity among the explanatory variables, which weakens the statistical power and interpretability of individual factor loadings. In this context, the size factor is not statistically significant, while the value factor is negative, pointing to a growth-oriented exposure. The estimated market beta of 0.64 is therefore not considered fully representative of the company's underlying risk profile, as TPRO operates in the semiconductor industry, which is structurally more cyclical and volatile than the broad equity market and would be expected to exhibit a beta above 1.

CAPM: regression approach

Using the traditional CAPM with STOXX 600 returns, we obtained a beta of 0.85. While higher than the Fama–French market beta, this estimate still appears downward biased.

CAPM: Peer-based Beta

Finally, considering that TPRO has no effective financial debt, we deemed it appropriate not to apply the Hamada relevering approach and to assume that the levered beta is equal to the unlevered beta. Accordingly, we derived the unlevered beta as the median of the peer group betas, consistently extending the net debt free assumption to the comparable companies. This results in a beta of 1.33, which we adopt for the computation of the cost of equity, as it appropriately reflects the underlying business risk of the semiconductor sector without introducing distortions related to financial leverage.

Avg. 3 years	Advantest	BE Semiconductor	Chunghwa Precision	FormFactor	MJC	MPI	Teradyne	VAT Group	WinWay Tech.
Beta Levered	1.31	1.44	1.14	1.73	1.33	1.26	1.50	1.13	1.37

Source: FactSet, Team Elaboration

Risk-Free Rate

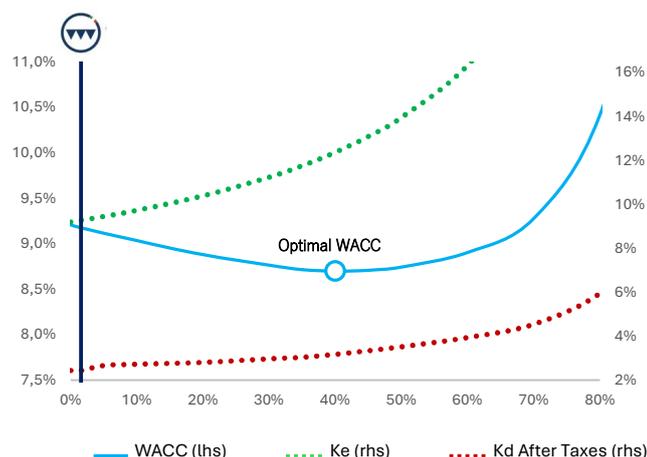
We adopted the yield of the 10-year German government bond (2. as a proxy for the risk-free rate, ensuring consistency with the euro-denominated cash flows considered in the analysis. (FactSet, updated 27/01/26).

Equity Risk Premium

The Equity Risk Premium (ERP) has been estimated starting from the 2025 implied ERP provided by A. Damodaran (January 2026) and subsequently adjusted by adding a country risk premium, weighted according to TPRO's geographic revenue exposure across the countries in which it mainly operates (USA, Taiwan, South Korea, Europe). The resulting ERP amounts to 4.77%

WACC OPTIMIZATION

Given TPRO's structurally low financial leverage and solid cash position, we assessed the capital structure that minimizes the Company's WACC and, in turn, maximizes enterprise value. We analyzed the sensitivity of the cost of equity, cost of debt and overall WACC to different D/(D+E). In our analysis, we assumed a stable corporate tax rate of 25% and a beta unlevered of 1.33. The cost of equity was estimated by relevering the unlevered beta across different leverage scenarios, capturing the progressive increase in equity risk as financial leverage rises. The cost of debt was derived by adding an appropriate credit spread to the risk-free rate, based on the implied interest coverage ratio (ICR) associated with each leverage level, in line with Damodaran's synthetic rating framework. As leverage increases, the Company's credit profile deteriorates, resulting in higher spreads and a rising after-tax cost of debt. Combining these assumptions, we find that TPRO's WACC follows a U-shaped profile, decreasing initially as moderate leverage lowers the weighted cost of capital, before increasing again as higher financial risk outweighs the tax shield benefits. Our analysis indicates an optimal WACC of 8.73% resulting in a 52bps decrease compared to current WACC of 9.21%, with a D/(D+E) in the range of 35% and 45%. From this result, we deduce that the current D/(D+E) ratio of 1.55% is suboptimal, and a different capital structure could enhance the enterprise value without materially compromising the Company's credit quality.



Source: FactSet, Team Elaboration

DCF

€m]	FY2024	FY2025E	FY2026E	FY2027E	FY2028E	FY2029E	FY2030E	FY2031E	FY2032E	FY2033E	FY2034E	FY2035E	TV
Revenues	543.2	626.6	754.6	937.4	1,172.5	1,466.4	1,793.0	2,049.4	2,283.4	2,494.2	2,684.1	2,857.6	-
Non-memory	479.2	501.6	616.1	754.8	907.6	1,080.6	1,274.7	1,452.9	1,611.0	1,747.6	1,862.9	1,958.6	-
Final Testing	64.0	125.0	123.6	132.7	142.5	153.0	164.3	175.2	185.8	195.9	205.5	214.6	-
Memory	-	-	15.0	50.0	113.4	211.4	303.2	355.2	400.7	439.1	470.6	495.7	-
Silicon Photonics	-	-	-	-	9.0	21.4	50.8	66.1	85.9	111.7	145.2	188.7	-
Growth [%]	32.71%	15.36%	20.43%	24.23%	25.08%	25.07%	22.27%	14.30%	11.42%	9.23%	7.61%	6.47%	-
EBITDA	136.5	217.4	301.8	393.7	445.5	586.6	753.1	840.2	959.0	1,072.5	1,154.2	1,228.8	-
EBITDAm	25.0%	34.7%	40.0%	42.0%	38.0%	40.0%	42.0%	41.0%	42.0%	43.0%	43.0%	43.0%	-
D&A	69.4	68.5	70.4	74.2	85.9	87.6	89.4	94.9	112.3	114.6	116.9	119.2	-
EBIT	67.1	148.9	231.4	319.5	359.6	498.9	663.7	745.3	846.7	957.9	1,037.3	1,109.6	-
Taxes	(34.2)	37.2	57.9	79.9	89.9	124.7	165.9	186.3	211.7	239.5	259.3	277.4	-
NOPAT	-	111.7	173.6	239.7	269.7	374.2	497.7	559.0	635.0	718.4	778.0	832.2	-
Net CapEx	-	50.0	107.0	143.0	93.8	95.7	152.7	188.7	122.6	125.1	127.6	130.1	-
NWC	156.4	180.5	217.3	270.0	337.7	422.3	516.4	590.2	657.6	718.3	773.0	823.0	-
Change NWC	-	24.0	36.9	52.7	67.7	84.7	94.0	73.8	67.4	60.7	54.7	50.0	-
FCFF	-	106.2	100.1	118.2	194.1	281.5	340.4	391.4	557.3	647.2	712.6	771.3	-
Disc. FCFF	-	-	100.1	108.2	162.8	216.1	239.3	251.9	328.5	349.3	352.2	349.0	6,886.2

WACC	Terminal growth (g)	Enterprise Value [€m]	Net Cash Position [€m]	Equity Value [€m]	Outstanding shares (m)	Target Price [€/sh]
9.21%	4.00%	9,343.7	(704.0)	1,004.8	656.3	15.38

Source: Team Elaboration

Growth Rate

The long-term growth rate is based on five-year FactSet consensus forecasts for expected inflation and real GDP. A revenue-weighted real GDP across operating geographies implies 4.4%; a conservative 4.0% was assumed, aligned with expected inflation plus U.S. real GDP, reflecting market maturity.

Monte Carlo Simulation



In order to assess the sensitivity of TPRO target price against the main valuation risks, we performed a Montecarlo simulation stressing each of our core assumptions around its base case. So on seven variables, including revenue CAGR (Logic, HBM, Final Testing, SiPh), EBITDA margins (FY26E-35E), WACC and Terminal Growth Rate. Results show that: (i) 75% of TP outcomes support a HOLD recommendation, with only 17% and 8% of outcomes supporting a SELL and a BUY, respectively and (ii) the most sensitive variable is represented by YoY Logic segment Revenues Growth (Tornado chart), followed by YoY HBM segment Revenues Growth. To accurately reflect TPRO's cost structure, we integrated a dynamic adjustment model for EBITDA margins within our Monte Carlo simulation. Specifically, our model accounts for operating leverage by applying a +/- 400 bps variance to the base-case EBITDA margin, contingent on whether the simulated revenue outperforms or underperforms our central projections. This sensitivity is particularly critical as fixed-cost absorption remains a key driver of TPRO's profitability. For revenue inputs, we assigned a distinct beta distribution to each segment, reflecting different levels of forecast uncertainty. Annual growth rates were modelled by scaling base-case assumptions with random draws from the respective beta distributions, ensuring economically coherent growth paths across simulations.

Variable	Distribution	Upper-Lower
Revenue YoY Growth Logic	Beta	0.8 ; 1.2
Revenue YoY Growth HBM	Beta	0.75 ; 1.25
Revenue YoY Growth SiPh	Beta	0.7 ; 1.3
Revenue YoY Growth FT	Beta	0.85 ; 1.15
EBITDA margin	Beta	Based on Total Revenues
WACC	Uniform	8.71% ; 9.71%
g	Truncated Normal	3.56% ; 4.44%

Scenarios

We developed bull and bear-case scenarios for TPRO by adjusting growth and market penetration assumptions while preserving a consistent economic rationale. Extreme outcomes are instead captured through the Monte Carlo stress test. The resulting scenarios remain coherent with our investment thesis, with the bull case implying a 25% upside and the bear case a 17% downside, supporting our **HOLD recommendation**.

Bull Case

An Unchallenged Leadership

In the logic market, TPRO remains the undisputed leader, preserving a 60% market share and dominating the high-margin HPC and AI segments. FormFactor is able to offer resistance only in the consumer segment, while other Taiwanese players, exposed to consumer demand and ASIC testing for Vertical MEMS, fail to keep pace and are progressively cannibalized.

Chasing Ambitious Goals

The entry into HBM and silicon photonics proves successful from 2028 onward, with meaningful market share in the former and an exceptionally high CAGR in the latter. The adoption of Vertical MEMS for memory testing becomes a key differentiator, while the ability to integrate this technology with optical testing represents an additional driver of success.

Scaling Without Breaking

Heavy but necessary capex does not translate into a long-term operational burden; instead, it enables organic growth while preserving best-in-class EBITDA margins, returning close to the 2022 peak of 45% despite the more dilutive nature of the new segments

A Mature Company... with Room to Grow

With no significant impact from China on the TAM and supported by the rapid expansion of high-potential technologies such as silicon photonics, TPRO continues to grow and remains well positioned to capture future industry trends and growth opportunities.

Bear Case

Challenging the King

FormFactor and Taiwanese competitors challenge TPRO in Vertical MEMS, triggering a price war in the ASIC and consumer segments where, despite the use of MEMS technologies, complexity is not a key differentiator. While TPRO manages to retain its leadership in the AI segment, MEMS market share comes under pressure.

Sometimes a Dream Remains Just That

HBM adoption of MEMS technologies is delayed, and competitors, leveraging their long-standing relationships with foundries, use the additional time to execute the required technological upgrades without difficulty. Silicon photonics is once again postponed, dampening previously built expectations.

The Decline of a Kingdom

In the absence of new disruptive technologies and China capturing an increasing share of the TAM, TPRO finds itself lacking high-growth segments and burdened by a heavy structure, as past expansions fail to deliver expected returns, leading to EBITDA margin decline.

Relative Valuation

To capture the market’s perspective, we conducted a relative valuation based on a selected peer group across the semiconductor test and interconnect value chain. **In probe cards and test interfaces**, the peer set includes Advantest, Chungwa Precision Test, FormFactor, Micronics Japan Co., MPI Corporation, Teradyne, and WinWay Technology, while BE Semiconductor and VAT Group are included for their **exposure to adjacent segments such as advanced packaging, back-end equipment, and high-precision components**. Together, these companies offer a comprehensive view of global leaders across probe cards, ATE, packaging, back-end processes, and metrology, reflecting the innovation and technological leadership driving the market. This peer framework provides a robust reference for assessing Technoprobe’s relative valuation.

Company	Country	Mkt Cap 2024A [€m]	Revenues 2024A [€m]	Profitability		Growth	Risk	Cash Generation	Value Drivers*			Comparables
				EBITDA margin 2024A	ROCE 2024A				EBITDA CAGR 2024A	D/E	CFO/Curr.Liab. 5y Avg	
Technoprobe	IT	3,753	543	25%	6%	30%	0.02	90%	●●●	●●	●●●	TARGET
ACM Research A	US	913	723	21%	11%	35%	0.21	18%	●●	●●●	●●	X
Advanced Energy Inds	US	4,207	1,370	9%	3%	22%	0.56	55%	●	●●●	●●	X
Advantest	JP	43,302	4,764	36%	31%	24%	0.18	88%	●●	●●	●●●	✓
Aixtron	DE	1,727	633	22%	13%	19%	0.01	-5%	●	●●●	●	X
ASM International	NL	27,565	2,933	34%	20%	12%	0.01	77%	●	●●●	●●●	X
BE Semiconductor	NL	10,736	608	37%	21%	58%	1.09	135%	●●●	●●	●●●	✓
Camtek	IL	3,539	397	28%	17%	11%	0.38	81%	●●	●●	●●●	X
Chroma ATE Inc.	TW	5,124	622	29%	21%	35%	0.16	48%	●●	●●	●●	X
Chungwa Precision Test	TW	852	104	26%	7%	32%	0.00	100%	●●●	●●●	●●●	✓
Cohu	US	1,202	371	-5%	-8%	65%	0.04	21%	●●	●●●	●●	X
Entegris	US	14,445	2,996	29%	4%	11%	1.10	129%	●	●●	●●	X
FormFactor	US	3,291	706	11%	7%	27%	0.04	102%	●●●	●●●	●●●	✓
J.E.M.	JP	169	146	24%	11%	2%	0.21	28%	●●●	●●	●●	X
KLA Corp.	US	81,395	9,058	43%	30%	11%	2.02	106%	●	●●●	●●●	X
Kulicke and Soffa Inds	US	2,417	652	-3%	-6%	131%	0.04	76%	●●●	●●●	●	X
Leeno Industrial	KR	1,916	189	50%	19%	21%	0.00	375%	●●●	●	●●●	X
Micronics Japan Co.	JP	929	340	27.7	19%	33%	0.02	48%	●●●	●●	●●●	✓
MPI Corporation	TW	2,570	293	30%	23%	41%	0.25	42%	●●●	●●	●●●	✓
Onto Innovation	US	7,950	913	28%	11%	24%	0.01	122%	●●●	●●	●●	X
Photronics, Inc.	US	1,441	798	35%	12%	-7%	0.02	118%	●●●	●	●●	X
Teradyne	US	19,805	2,603	24%	20%	31%	0.03	118%	●●	●●●	●●	✓
Ultra Clean Holdings, Inc.	US	1,564	1,939	8.0	76	30%	0.11	23%	●●	●	●●	X
VAT Group	CH	10,959	989	32%	24%	21%	0.32	101%	●●	●●	●●	✓
Veeco Instruments	US	1,470	663	14%	7%	21%	0.41	31%	●	●●●	●●	X
WinWay Technologies	TW	1,181	167	28%	25%	35%	0.05	76%	●●●	●●	●●●	✓
Yamaichi Electronics CO., Ltd.	JP	311	277	25%	13%	6%	0.16	71%	●●	●	●●	X

*Qualitative alignment is rated on a three-level scale: (●●●) best-in-class, (●●) strong alignment, and (●) marginal relevance.

Source: FactSet, Team Elaboration

Our relative valuation initially considered both EV/EBITDA and EV/CE multiples to capture different perspectives on value: EV/EBITDA reflecting operating performance and medium-term growth, and EV/CE reflecting capital efficiency. Given the highly capital-intensive nature of semiconductor testing and interconnect companies, we expected this second multiple to better represent how effectively firms allocate and deploy capital. Based on this reasoning, EV/CE was selected as the primary reference multiple and applied to TPRO’s forward fundamentals to derive the market-based valuation benchmark.

Company	Ticker	FY Ending Month	DISCARDED MULTIPLE		First Regressor		Second Regressor	SELECTED MULTIPLE		Regressor	
			EV/EBITDA 2025E	EV/EBITDA 2026E	EBITDA margin 2025E	EBITDA margin 2026E	EBITDA CAGR 2025E-27E	EV/CE 2025E	EV/CE 2026E	ROCE 2025E	ROCE 2026E
Advantest	6857-JP	March	39.7x	30.3x	35.6%	43.3%	26.0%	28.6x	24.5x	66.5%	73.3%
BE Semiconductor	BESI-NL	December	54.6x	41.9x	36.9%	34.0%	59.1%	10.5x	14.1x	16.5%	30.7%
Chungwa Precision Test	6510-TW	December	47.1x	42.6x	26.1%	31.7%	31.9%	8.1x	8.8x	13.2%	18.4%
FormFactor	FORM-US	December	30.1x	36.5x	11.1%	17.5%	25.5%	4.0x	5.9x	9.6%	13.4%
Micronics Japan Co	6871-JP	December	13.3x	10.7x	27.7%	28.6%	34.5%	5.2x	5.8x	27.5%	31.6%
MPI Corporation	6223-TW	December	48.4x	35.6x	29.9%	34.9%	45.1%	18.1x	15.8x	31.8%	41.2%
Teradyne	TER-US	December	39.8x	34.7x	23.7%	25.2%	31.4%	10.0x	12.0x	20.7%	31.0%
VAT Group	VACN-CH	December	37.2x	41.4x	31.6%	30.3%	21.3%	10.7x	13.5x	24.9%	28.5%
WinWay Technologies	6515-TW	December	42.8x	39.5x	27.7%	30.1%	37.2%	15.8x	17.5x	33.8%	41.2%
AVG			39.2x	34.8x	27.8%	30.6%	34.7%	12.3x	13.1x	27.2%	34.4%
MEDIAN			39.8x	36.5x	27.7%	30.3%	31.9%	10.5x	13.5x	24.9%	31.0%

Source: FactSet, Team Elaboration

This intuition is confirmed by our regression analysis across the peer group. EV/EBITDA shows very low explanatory power when regressed against EBITDA margin and EBITDA CAGR over 2025–2027E, while EV/CE exhibits strong statistical significance against forward-looking ROCE, confirming that market valuations are primarily driven by capital efficiency and validating its use as the reference multiple. Applying the regression-implied EV/CE to TPRO’s 2026E fundamentals results in a market-based equity value of **€15.83 per share**, which serves as the benchmark for our relative valuation.

Multiple (y)	Regressor	Year	Slope	Intercept	R ²	Implied Multiple	EV [€m]	NFP [€m]	# Shares [m]	Price per Share [€]
EV/EBITDA	EBIDA margin 2025	2025	63.77	21.50	0.16	-	-	-	-	-
	EBITDA margin 2026	2026	0.05	34.78	0.00	-	-	-	-	-
EV/EBITDA	EBITDA CAGR 2025E-27E	2025	53.19	20.80	0.06	-	-	-	-	-
		2026	10.53	31.15	0.02	-	-	-	-	-
EV/CE	ROCE 2025	2025	40.94	1.23	0.83	5.48	7206	(697)	653	12.10
	ROCE 2026	2026	30.86	2.50	0.80	6.71	9550	(789)	653	15.83

Source: FactSet, Team Elaboration

9. Environmental, Social & Governance (ESG)

To assess TPRO's ESG performance, we employ a **proprietary relative benchmarking methodology**. Instead of evaluating the company against a broad industry pool, we segment comparable peers into three distinct groups: **(i) pure players** in the probe card market, **(ii) large ecosystem leaders** with significant global market positions, and **(iii) European peers** operating under similar regulatory environments. For each group, we identify the most relevant ESG metrics, ensuring comparisons are meaningful and reflective of operational, social, and governance realities. By analyzing TPRO's performance relative to the group-specific industry averages, as well as best and worst performers, we derive weighted scores across Environmental, Social, and Governance pillars. This approach allows for a nuanced and tailored assessment, providing a clearer picture of the company's ESG positioning within each competitive context.

(I) PURE PLAYERS – weight 45%

This selection includes TPRO's **most direct competitors in the probe card and advanced testing interface markets**. We have chosen this group to isolate TPRO's performance against companies sharing nearly identical industrial structures and technological complexities, making the operational comparison highly significant. Consequently, the selected metrics focus on resource efficiency and human capital: carbon, water, and energy intensity (benchmarked against revenue) allow for an assessment of who possesses the most sustainable production model for a given output. In parallel, gender diversity and R&D intensity reflect the ability to attract and retain specialized STEM talent in a highly competitive market niche.

	Metric	Computation	Unit of Measure	TPRO 2024	Industry 2024	Best 2024	Worst 2024	Score	Weight	Pillar Score
E	Carbon Intensity	GHG Emissions (Scope 1+2) / Total Revenue	[tCO2e / €m]	56.1	68.0	29.9	159.8	8.0	40%	8.6
	Water Intensity	Total Water Withdrawal / Total Revenue	[m ³ / €m]	333.3	706.0	111.2	2073.3	8.9	40%	
	Energy Intensity	Total Energy Consumption / Total Revenue	[MWh / €m]	92.7	158.1	73.4	289.7	9.1	20%	
S	Female Employees	Female Employees / Total Employees * 100	[%]	34.1%	29.4%	44.6%	19.5%	5.8	60%	4.3
	R&D Intensity	R&D Intensity / Total Revenue * 100	[%]	9.7%	13.1%	23.6%	6.0%	2.1	40%	
G	Board Independence	Independent Directors / Total Board Members * 100	[%]	50.0%	48.8%	62.5%	33.3%	5.7	70%	6.1
	Anti-Corruption	Presence of a formal Anti-Corruption Policy	[T/F]	TRUE	100% T - 0% F	TRUE	TRUE	7.0	30%	

Source: Company Data, Team Elaboration

(II) ECOSYSTEM LEADERS – weight 25%

This pool features Advantest and Teradyne, the **"titans" of the semiconductor testing ecosystem**, selected because they represent the ESG gold standard for Tier-1 institutional investors. Comparing TPRO with these leaders is essential to evaluate whether Technoprobe is ready to attract large-scale international capital by aligning with those who hold dominant market shares. For this reason, the chosen metrics focus on supply chain responsibility and advanced governance: Scope 3 transparency and the Supplier Code of Conduct measure oversight of a complex global supply chain. Furthermore, the adoption of international frameworks (SASB, TCFD) and remuneration linked to ESG targets certify the company's commitment to global-level transparency.

	Metric	Computation	Unit of Measure	TPRO 2024	Industry 2024	Best 2024	Worst 2024	Score	Weight	Pillar Score
E	Scope 3 Transparency	Scope 3 Reported Value / Total Revenue	[tCO2e / €m]	153.9	449.4	102.9	796.0	9.3	100%	9.3
S	SCoC	Presence of formal Supplier Code of Conduct	[T/F]	T	100% T - 0% F	TRUE	TRUE	7.0	30%	6.5
	Management Diversity	Female Managers / Total Managers * 100	[%]	15.0%	14.2%	19.0%	9.4%	5.8	40%	
	Community Donations	Explicit Community Donation History	[T/F]	T	100% T - 0% F	TRUE	TRUE	7.0	30%	
G	ESG-Linked Pay	Presence of ESG targets in Remuneration Report	[T/F]	T	0% T - 100% F	FALSE	FALSE	10.0	50%	9.0
	Framework Alignment	Adoption of SASB, TCFD, and SBTi standards	[Count / T/F]	3/3	2.5/3	3/3	2/3	8.0	50%	

Source: Company Data, Team Elaboration

(III) EUROPEAN PEERS – weight 30%

This group includes **high-margin, high-precision European peers** that operate under the same regulatory perimeter as TPRO, including the CSRD and EU Taxonomy directives. We have selected these peers as they represent European excellence in transparency and corporate governance, serving as the ideal benchmark for regulatory compliance. The selected metrics – such as Taxonomy alignment and the renewable energy mix – directly measure the company's readiness for upcoming European sustainability mandates. Finally, indicators like the Gender Pay Gap and Board Diversity highlight the commitment to social and diversity standards that are now considered critical prerequisites in the continental tech market.

	Metric	Computation	Unit of Measure	TPRO 2024	Industry 2024	Best 2024	Worst 2024	Score	Weight	Pillar Score
E	Taxonomy Alignment	Taxonomy Aligned Revenue / Total Revenue * 100	[%]	0.0%	41.5%	83.0%	0.0%	2.0	60%	0.0
	Renewable Mix	Renewable Energy Consumption / Total Energy Consumption * 100	[%]	1.5%	89.3%	93.0%	85.6%	2.0	40%	
S	Gender Pay Gap	(Avg. Male Pay - Avg. Female Pay) / Avg. Male Pay	[%]	29.0%	14.0%	5.0%	23.0%	2.0	60%	0.0
	Avg. Training Hours	Total Training Hours / Total Employees	[Hours/FTE]	24.5	32.0	34.0	30.0	2.0	40%	
G	Board Independence	Independent Directors / Total Board Members * 100	[%]	50.0%	100.0%	100.0%	100.0%	2.0	30%	4.0
	Board Diversity	Female Board Members / Total Board Members * 100	[%]	20.0%	32.5%	40.0%	25.0%	2.0	30%	
	CSRD Readiness	Verification of report alignment with ESRS standards	[T/F]	T	100% T - 0% F	TRUE	TRUE	7.0	40%	

Source: Company Data, Team Elaboration

To determine the definitive ESG profile, we **aggregate the scores obtained in each individual pool** to calculate a final numerical value for the Environmental (E), Social (S), and Governance (G) pillars. This is achieved through a weighted average, where each pool is assigned a specific weight: 45% for Pure Players, 25% for Ecosystem Leaders, and 30% for European Peers. These weights prioritize direct operational comparison while still factoring in global institutional standards and regional regulatory excellence. The resulting numerical scores are then mapped onto the LSEG qualitative grading scale, which translates the quantitative performance into standardized letter ratings to identify TPRO's specific ESG performance class.

ENVIRONMENT	SOCIAL	GOVERNANCE
B	C	B

The results of our benchmarking analysis yield a final ESG evaluation of **"B"** for both the Environmental and Governance pillars, while the Social pillar receives a **"C"** rating. It is crucial to highlight that these scores are significantly tempered by the direct comparison with best-in-class European peers, whose established leadership in disclosure and sustainability mandates sets a high bar that TPRO is only now beginning to approach. This outcome underscores the **undergoing transformation** of the Company's institutional profile as it transitions toward greater maturity. While Technoprobe demonstrates solid performance in resource efficiency and a strengthening governance framework, the lower rating in the Social dimension reveals clear areas for improvement, particularly regarding **gender pay equity** and the **depth of employee training** compared to regional standards. Addressing these social metrics will be essential for TPRO to further elevate its sustainability profile and fully align with the leading ESG practices of its continental competitors.

10. Board of Directors Composition

Full name	Offices	Family Member	In charge since	N° of other offices	Committee			Background
					Control, Risk & Sustainability	Appointments & Remuneration	Related Party Transaction	
Cristiano Crippa	Chairman (Executive)	✓	1995 (Founder)	1				<ul style="list-style-type: none"> Co-Founder of TPRO Led growth from startup to global player
Roberto Crippa	Vice Chairman (Executive)	✓	2013 (Director since 1999)	2				<ul style="list-style-type: none"> Chemical engineer focused on R&D Holder of multiple international patents
Stefano Felici	CEO (Executive)	✓	2017 (Joined in 2008)	1				<ul style="list-style-type: none"> PhD in Electronic Engineering Former head of U.S. operations and global sales
Giulio Sirtori	Lead Independent Director		02/05/2023 (Listing)	2	✓	President		<ul style="list-style-type: none"> GM of Confindustria Lecco e Sondrio Management & institutional relations expert
Susanna Pedretti	Independent non-Executive		02/05/2023 (Listing)	3	President	✓	✓	<ul style="list-style-type: none"> Corporate governance and compliance lawyer Chair of supervisory bodies (ODV)
Elisabetta Cugnasca	Independent non-Executive		02/05/2023 (Listing)	2	✓	✓	✓	<ul style="list-style-type: none"> Bocconi Economics graduate, ex-auditor Investor relations and internal audit specialist
Antonio Sanna	Independent non-Executive		24/04/2024 (Renewal)	1			President	<ul style="list-style-type: none"> Former General Counsel (Acea, Autostrade) Corporate legal and regulated-sector expert
Gregory Stephen Smith	Non-Independent non-Executive		27/05/2024 (Co-opted)	1				<ul style="list-style-type: none"> CEO of Teradyne 30+ years in semiconductor test equipment
Carlos Ortega Arias Paz	Independent non-Executive		29/04/2025 (Assembly)	4				<ul style="list-style-type: none"> Harvard MBA, Co-CEO of Alba Expertise in strategic finance and investments
Chih-Kuang Yang	Non-Independent non-Executive		10/07/2025 (Expansion)	1				<ul style="list-style-type: none"> CEO of Yee Wei Inc. GM of TPRO Taiwan Asian market and semiconductor expertise

Source: Company Data

11. Production Capacity Bottleneck – Proprietary Model

$$\text{Annual Good Probe Cards Produced}_{2025} = C \times H_{\text{annual}} \times M \times U \times (1 - S)$$

Where P represents effective annual production, C the hourly production per machine, H_{annual} the total annual operating hours per machine, M the number of machines, U the machine utilization rate, and S the scrap rate.

$$330 [\text{probe/hour/machine}] \times 8736 [\text{h/year}] \times 60 [\text{machines}] \times 0.9 [\text{utilization rate}] \times (1 - 0.03) [\% \text{ good parts}] = 151,005,254 [\text{probe/year}]$$

Our proprietary model estimates TPRO's **maximum achievable revenues** through 2035 under a high but sustainable production **utilization rate of 90%**, identifying the revenue level that **cannot be exceeded** due to physical capacity constraints. Revenues are derived from current production capacity and average selling prices of probe cards, assuming that 60% of total revenues come from direct probe card selling and 40% from repair, engineering and service activities. The resulting estimate is consistent with 2025E revenues of €303 million (excluding final testing activities). The analysis shows that TPRO is **already operating at full capacity, limiting short-term revenue upside** despite continued demand growth until the new manufacturing facility becomes operational in 2028. The model also captures **profitability dynamics** by linking margins to capacity utilization: **operating efficiency** and marginality improve when **utilization lies in the 80–90%** range, which we identify as the **optimal operating zone**.

	2026E	2027E	2028E	2029E	2030E	2031E	2032E	2033E	2034E	2035E
Production Capacity [m probe/year]	174	209	303	332	381	467	476	486	496	500
<i>Growth Rate</i>	15%	15%	100%*	10%	20%	40%	2%	2%	2%	1%
Average Selling Price [constant growth 5% YoY]	€ 2.10	€ 2.21	€ 2.38	€ 2.50	€ 2.63	€ 2.76	€ 2.89	€ 3.04	€ 3.19	€ 3.35
Revenue at full capacity [€m]	€ 365	€ 460	€ 721	€ 832	€ 1,001	€ 1,287	€ 1,379	€ 1,477	€ 1,582	€ 1,677
Tot. Expected Revenue [€m] (without final testing)	€ 631	€ 815	€ 1,030	€ 1,313	€ 1,628	€ 1,874	€ 2,097	€ 2,298	€ 2,478	€ 2,643
<i>Of which from direct selling (60%)</i>	€ 378	€ 489	€ 618	€ 788	€ 977	€ 1,112	€ 1,258	€ 1,379	€ 1,487	€ 1,585
Utilization Rate	93%	95%	77%	85%	88%	78%	83%	84%	85%	85%

* Growth related to 2025 capacity

Growth Source: Company Data, Team Elaboration

12. Geographical Risks

Taiwan

Over the years, Taiwan has developed a highly competitive probe card ecosystem, intensifying pressure on TPRO. The company faces two main structural risks: (i) **TSMC's dual role as both a key customer and a technology conduit to competitors**, as probe cards supplied by TPRO are analysed through collaboration with **CHPT**, a domestic probe card manufacturer and direct competitor, enabling lower-cost alternatives – particularly in mid- to lower-end segments where price sensitivity is higher; and (ii) **aggressive expansion by MPI Corporation**, which is actively growing its MEMS probe card production while facing patent infringement allegations, highlighting a competitive environment that is both intense and, at times, potentially unfair. In this context, TPRO's strategic agreement with MS Sun and WinWay is designed to safeguard core technologies: WinWay is authorised to assemble, sell, and service the company's products under strict controls, reducing replication risk and know-how leakage while maintaining market access in Taiwan.



China

China is rapidly closing the gap with global semiconductor leaders, driven by the speed, scale, and centralized coordination of its industrial initiatives. The country is building a more **self-sufficient semiconductor ecosystem** by combining strategic control over critical inputs, such as rare earths, with assertive state-led policies. The launch of **Big Fund III (c. USD 47–48bn)** aims to accelerate substitution of restricted foreign technologies across the value chain. Huawei has emerged as a central orchestrator, restructuring its supply chain through initiatives like "Spare Tire" to reduce reliance on U.S. technologies while developing domestic **AI compute solutions**, including the CloudMatrix 384 platform. Strategic urgency is underscored by disruptions in Nvidia's ecosystem, where suppliers for H200 chips reportedly suspended production after Chinese customs blocked entry. This push extends into testing and validation infrastructure, a critical bottleneck. In the probe card segment, **MaxOne** is emerging as a key domestic player, leveraging MEMS capabilities, alignment with China's semiconductor roadmap, SMIC's 7nm expansion, and state-backed support to supply test solutions for advanced AI chips, gradually exerting price-based pressure on Taiwanese suppliers and integrating AI compute, fabrication, and testing into a cohesive domestic strategy.

