CFA Institute Research Challenge

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Team Short Management

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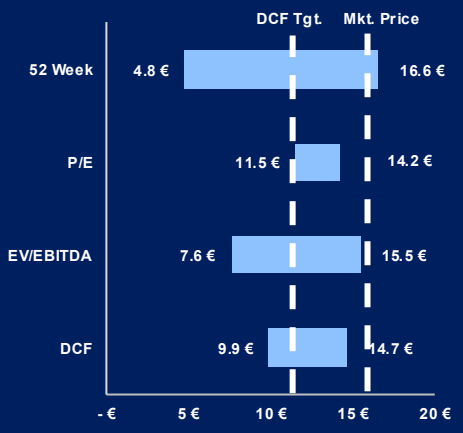
CFA Italian Research Challenge
Initial Coverage | January 31st 2026

SELL

Price: €15.63
Target Price: €11.83
Downside: -24.3%

Valuation



Market Data

Last Close	€15.63
Market Cap	€10.01bn
Shares Out.	640.32mn
Avg. Volume	700.24k
52-Week High	€16.60
52-Week Low	€4.77
Last Updated	Jan 30 2026
Listed On	Euronext Milan
Bloomberg	TPRO IM
Reuters	TPRO.MI
Industry	Technology, Tech Hardware & Semiconductors

TR in 3y: 227.4% vs. 170.8% FTSE MIB

Source: FactSet

Technoprobe (TPRO) is a leading supplier of semiconductor test interfaces, focused on probe cards used in wafer-level testing of advanced logic chips. Founded in 1996 by the Crippa family and first listed on Euronext Growth Milan in 2022, the company competes in the €2.1bn semiconductor probe card market. In FY-24/H1-25, TPRO generated €543mn/€329mn of revenue, resulting in €137mn/€106mn of EBITDA.

Priced for Perfection with Little Room for Error

We initiate the coverage of Technoprobe with a SELL recommendation and a target price of €11.8 per common share, offering a 24.3% downside. We believe TPRO is priced for perfection with little-to-no margin for error on execution:

a) The recent rally in the stock reflects growing enthusiasm among investor on the potential for TPRO to become a meaningful memory test supplier in the HBM market. **However, we believe the company lacks qualification progress, domain expertise and acknowledges weak visibility in the market.** This is underpinned by the company's commentary that **gaining meaningful HBM memory-test share will be difficult, uneven and margin-dilutive in the coming years.**

b) We believe **TPRO's strategy of moving downstream to the more commoditized and lower margin final testing through acquisitions has a similar "margin-cap"**, as even with increased complexity in final testing, volumes should be moving upstream in the testing process due to packaging trends. This is because advanced packaging increases the value of KGD.

c) Upcoming earnings (Q4-25, Q1-26) should **raise concerns among investors on the pace of the HBM adoption**, as FORM will show increasing HBM related revenues, while TPRO's numbers will reflect slower progress and a more disappointing margin trajectory. Additionally, the current price discounts aggressive growth assumptions in outer-years, leading to **much of the equity value being tied up in the terminal value.** These growth assumptions could quickly shift as the HBM shortage reverses, and the order book deflates, similar to the 2022-23 demand stagnation in the semiconductor market.

From Great to Good: Catalysts and Signposts

In the coming months, TPRO is set to release their FY-25 results, which should lead to a revision of margin expectations due to increased spend on, but no meaningful revenue contribution from HBM, and still lagging final testing. Additionally, the doubling of capacity emphasized by mgmt. has yet to start, which could introduce additional uncertainty around short-term share gains in the HBM segment.

On February 4th, 2026, FORM will announce Q4-25 results and likely provide a positive outlook on their HBM segment, which has been a key growth driver in recent quarters. Strong and persistent performance by FORM in this segment would also reflect lower upside for TPRO as they aim to take share in a market that already has a stable dual-sourcing model. **Over the next quarters, the market should realize that TPRO is a company that is moving from great to good**, as they shift away from their legacy, high-margin wafer-level advanced logic business to lower quality, more cyclical, and more competitive segments. This cyclicality is well reflected in the lower multiples of memory businesses such as Micron Technology and SK Hynix (13.3x and 6.8x, respectively vs. TPRO 103.0x).

Financials Highlights: Strong Growth, Little Upside

Our assessment of TPRO's business potential reflects significant revenue growth due to capacity expansion, yet we remain less optimistic relative to consensus. Despite the top-line growth, our EBITDA margin outlook reflects a target of 36.3% by FY-27, lower than the midpoint of guidance at ~39.0%. Our segment level revenue build shows that the lack of margin upside comes from slightly improving final testing margins at 20% as well as lower initial HBM margins at 36%. Additionally, while consolidated numbers in recent quarters may show strong growth, **organic growth in the core wafer-level segment has been lacklustre.**

Valuation & Forecasts

Our valuation reflects slower margin recovery and HBM ramp:

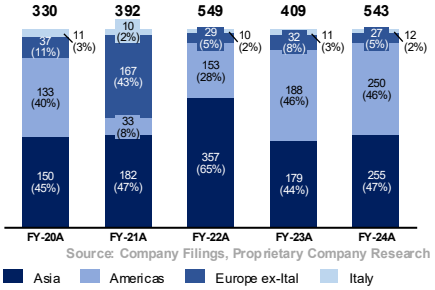
Fiscal Period	FY-25E	FY-26E	FY-27E	FY-28E	FY-29E	FY-30E
Revenue	**626.6**	**776.0**	**949.2**	**1,216.1**	**1,482.1**	**1,800.5**
Growth YoY	*15.4%*	*23.8%*	*22.3%*	*28.1%*	*21.9%*	*21.5%*
(-) Cost of Revenue	(345.9)	(370.0)	(441.3)	(537.1)	(624.6)	(731.8)
Gross Profit	**280.6**	**406.0**	**507.8**	**679.0**	**857.5**	**1,068.7**
Gross Margin	*44.8%*	*52.3%*	*53.5%*	*55.8%*	*57.9%*	*59.4%*
(-) Research & Development	(60.0)	(80.1)	(104.9)	(143.4)	(185.7)	(252.1)
(-) Sales, General & Administrative	(107.1)	(129.0)	(153.2)	(190.5)	(225.0)	(264.7)
(-) Net Impairment of Financial Assets	–	–	–	–	–	–
EBIT	**113.4**	**196.9**	**249.7**	**345.1**	**446.8**	**551.9**
EBIT Margin	*18.1%*	*25.4%*	*26.3%*	*28.4%*	*30.1%*	*30.7%*
(+) Other Income (Expenses), Net	0.6	0.7	0.9	1.1	1.4	1.7
(+) Finance Income	6.5	8.1	9.9	12.6	15.4	18.7
(-) Finance Expenses	(0.6)	(0.8)	(1.0)	(1.2)	(1.5)	(1.8)
(+) Foreign Exchange Gains (Losses)	1.5	1.8	2.2	2.9	3.5	4.2
Pre-Tax Profit	**121.4**	**206.7**	**261.7**	**360.5**	**465.6**	**574.7**
(-) Income Tax Expense	(29.1)	(49.6)	(62.8)	(86.5)	(111.7)	(137.9)
Net Income	*92.2*	*157.1*	*198.9*	*274.0*	*353.8*	*436.8*
(-) Attributable to Non-Controlling Interests	(1.0)	(1.0)	(1.0)	(1.0)	(1.0)	(1.0)
Net Income to Parent	91.2	156.1	197.9	273.0	352.8	435.7

BUSINESS DESCRIPTION

The Typical Semiconductor Test Flow – *Exhibit 1*

Source: Company Filings, Proprietary Company Research

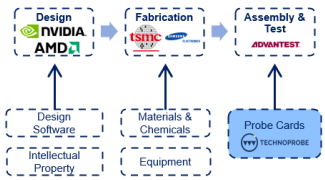
TPRO Revenues (mn€) by Region – *Exhibit 2*



Source: Company Filings, Proprietary Company Research

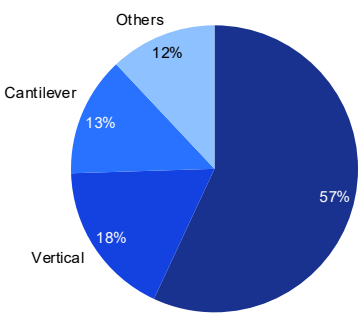
Probe Card: Hi-tech device for testing the functioning of chips during their construction process – *Exhibit 3*

Simplified Semiconductor Value Chain - *Exhibit 4a*



Semiconductor Players - *Exhibit 4b*

Logic Market Share – *Exhibit 5*



Source: World Semiconductor Trade Statistics

TPRO is an Italian semiconductor-equipment company that designs and manufactures probe cards. Probe cards are the custom electromechanical interfaces used to electrically test chips while they are still on the silicon wafer; because each chip design requires its own probe card, the business operates as a highly specialized, high-mix consumables model tied directly to semiconductor production volumes.

The company is the global leader in vertical MEMS probe cards for advanced logic, holding roughly 60% of the MEMS logic market and about 34% of total logic probe cards (including non-MEMS vertical and epoxy/cantilever).

Vertical MEMS is the most advanced probe-card architecture and is increasingly required at leading-edge nodes due to higher pin counts, rising power density, and stricter signal-integrity demands, all of which drive higher complexity and structurally higher ASPs. While historically concentrated in logic, TPRO is also expanding into High Bandwidth Memory (HBM), where advanced packaging flows and tighter Known Good Die requirements significantly raise test intensity, and it additionally participates in packaged-device final testing as a smaller complementary segment.

Customers and end markets: TPRO serves leading foundries, Integrated Device Manufacturers (IDMs), and Outsourced Semiconductor Assembly and Test providers (OSATs). Its largest exposure is to TSMC, which accounts for roughly 70% of revenue and manufactures chips for downstream customers such as Apple, Nvidia, and various AI-ASIC designers. In practice, these companies do not buy directly from TPRO; instead, demand flows through TSMC's wafer-testing needs, where probe cards must be designed, qualified, and delivered within a short turnaround cycle of only a few months to match each customer's tape-out schedule. FY24 revenue was ~49% Consumer (PC/smartphone), ~35% Data Center and AI, and ~14% Automotive and Industrial, with medium-term growth expected in the mid-single-digit range.

Footprint and acquisitions: TPRO operates a vertically integrated network across Europe, North America and Asia (23 legal entities). In 2024 it acquired Device Interface Solutions (DIS) from Teradyne, expanding from wafer-level probe cards into final-test interfaces. Unlike probe cards, which test chips while they are still on the wafer, final testing occurs after the chip is packaged, using a Device Interface Board (DIB) that links the finished component to the test machine to verify it works under real operating conditions. DIS contributed about €63m of revenue in 2024 on a partial-year basis (implying ~€135m annual run-rate) at ~15% EBITDA margin, well below the core probe-card business.

INDUSTRY OVERVIEW & COMPETITIVE ANALYSIS

THE SEMICONDUCTOR VALUE CHAIN

Over the past decade, the semiconductor industry has transitioned from vertically integrated companies into an ecosystem with many specialized players. Key participants in the industry include: **Chip designers** (e.g. NVIDIA, AMD): They design chip architectures (e.g. GPUs, CPUs, mobile SoCs, AI ASICs); **Foundries** (e.g. TSMC, Samsung Foundry, Intel) then manufacture the wafers into chips for end users, such as Apple; Die testing can be conducted internally, though at times foundries employ **Outsourced Assembly and Test (OSAT)** companies (e.g. ASE, Amkor). **Automatic Test Equipment (ATE) companies** (Teradyne and Advantest, at a 95% market share duopoly) provide the test machinery for chips.

COMPETITIVE DYNAMICS

A key component of ATE is the probe card, which is the customized physical and electrical connection between each die and ATE. There exists probe cards for logic dies, memory dies, silicon photonics dies, etc, but **Technoprobe currently only operates in the logic probe card market**. Within the logic probe card market, **Technoprobe only produces Vertical MEMS probes, which are the industry leading wafer test solutions used for the most demanding advanced-logic tests.**

Within **Vertical MEMS logic probing**, Technoprobe holds a **60%** share, while FormFactor holds the remaining **40%**, creating an effective duopoly in the highest-end subsegment. Customer qualification cycles for probe cards can take up to. Thus end customers tend to be "locked in" once they reach qualifications with a probe supplier.

Other probe-card vendors are based in Asia, and include Micronics Japan, Japan Electronic Materials, WinWay Technology, and MPI Corporation also manufacture probe cards, but are **currently 1-2 generations of technology behind** and are forced to produce **lower-margin, commoditized cantilever probe cards** for logic, memory, and final test. We estimate there to be a 5-10 year technology gap between Technoprobe and lower-end Asian manufacturers. We believe that Technoprobe currently has a strong technological moat in the near future. As Technoprobe currently is heavily engaged in new technological iterations for probe cards in HBM, final test, and ASICs, **we believe that the company will be able to maintain long term margin premiums.**

A weakness of Technoprobe, however, is the sales are highly concentrated. We estimate that **TSMC represents over 70% of revenues** (direct and indirect). This naturally forms high customer negotiating leverage, as reflected by the effects of TSMC-led dual sourcing requirements. Price pressure potential, however, is mitigated by lack of substitutes and qualification risks, and time-to-market constraints for TSMC, as well as TPRO develops non-logic probe cards in the future.

INDUSTRY OVERVIEW & COMPETITIVE POSITIONING

The Broader Industry Cycle

Porter's 5 Forces (appendix 2) – *Exhibit 6*

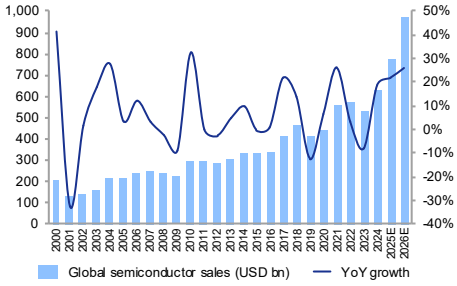
Source: team analysis

The testing probe market of TPRO is heavily correlated with the broader semis cycle. Historically, the semis cycle was dominated by supply dynamics. Long fab build times, chunky capacity adds, and pricing swings produced multi-year cycles (~4-6 years).

However, as the industry has become more modularized, cyclicality has become shorter, shallower, and demand driven. Downturns are increasingly about inventory corrections (order pushouts or cancellations to burn excess stock) and upturns are inventory rebuilds (restocking into improving demand). The **most recent industry downcycle (2022-2023)** was driven by consumer demand resetting following a post-covid surge, with global PC shipments falling 16.2% in 2022 and 14.8% in 2023. TPRO suffered a -26% decrease in revenue.

The semis industry is currently entering a new AI supercycle. Key drivers are growth are hyperscalers scaling AI compute, creating significant demand for leading-edge logic, memory, and silicon photonics chips. Concurrent to the increase in semiconductor chip demand, we also note a structural step up in testing due to chip complexity, thus unlocking a new growth driver for TPRO, with details mentioned below.

Global semiconductor market – *Exhibit 7*



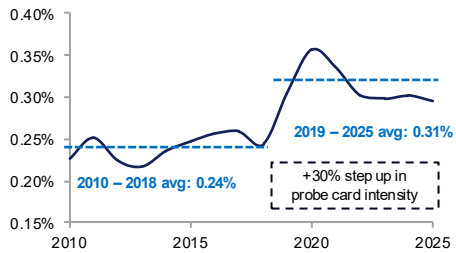
Source: World Semiconductor Trade Statistics

Structural Shifts within the Probe Card Market

AI/HPC CHIPS DRIVE CHIP COMPLEXITY

Leading-edge advanced logic devices (e.g. AI/HPC accelerators including Hopper/Blackwell, AMD Instinct Accelerators, Google TPUs) and other leading-edge logic devices have structurally increased test-interface requirements, with a **15-20x test intensity step-up compared to mobile SoCs**. New demands on probe cards include higher power delivery, thermal stability, tighter signal integrity, finer pitch and increased pin counts, and the **increased complexity continues to drive ASPs**. On the other hand, advanced logic testing faces constraints in scaling parallel testing due to system limitations and is a driver of testing probe volumes.

Probe card spend vs IC sales – *Exhibit 8*

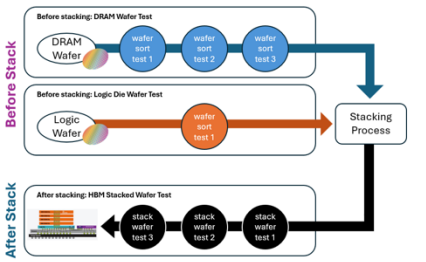


Source: FormFactor, TechInsights

HBM & ADVANCED PACKAGING UNLOCK NEW GROWTH LEVERS

Development of advanced packaging processes (e.g. 2.5D/3D multi-die integration) for advanced logic and memory (HBM3e, HBM4 and beyond) chips, as well as hybrid bonding techniques have increased the value of Known Good Die (KGD) yields. As a single bad die can compromise a multi-die assembly, the economic costs of a bad die increase with packaging complexity. This has pushed for greater wafer level (pre-packaging) screening, and the subsequent increase testing requirements and test intensity increases the amount of testing capacity necessary, with estimates that chiplet-based architecture could provide a 50% boost to the probe card opportunity. Advanced packaging also increases testing requirements downstream in final testing as system complexity increases non-linearly, with long term potential for uplift in margins.

HBM stack illustration – *Exhibit 9*

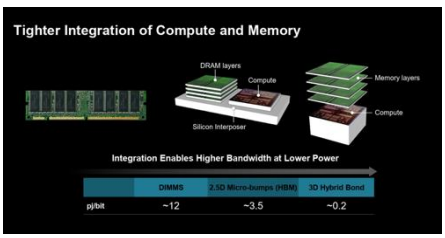


Source: Technoprobe, Formfactor

RISING VERTICAL INTEGRATION

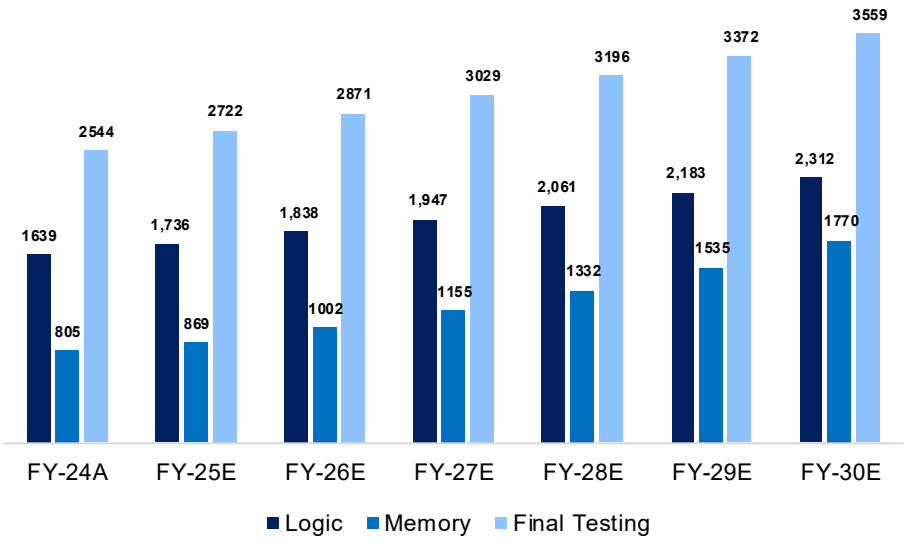
Rising device complexity is increasing the necessity for coordination across the testing value chain (ATEs, prober, probe cards) to co-optimize/validate semiconductor qualification cycles. Headline investments by ATE/OEMs in probe-card suppliers include Teradyne's 8% stake in Technoprobe, Technoprobe acquisition of DIS, etc. Tighter co-development and longer qualifications can support higher switching costs and reinforce incumbent positioning.

2.5D & 3D architecture – *Exhibit 10*

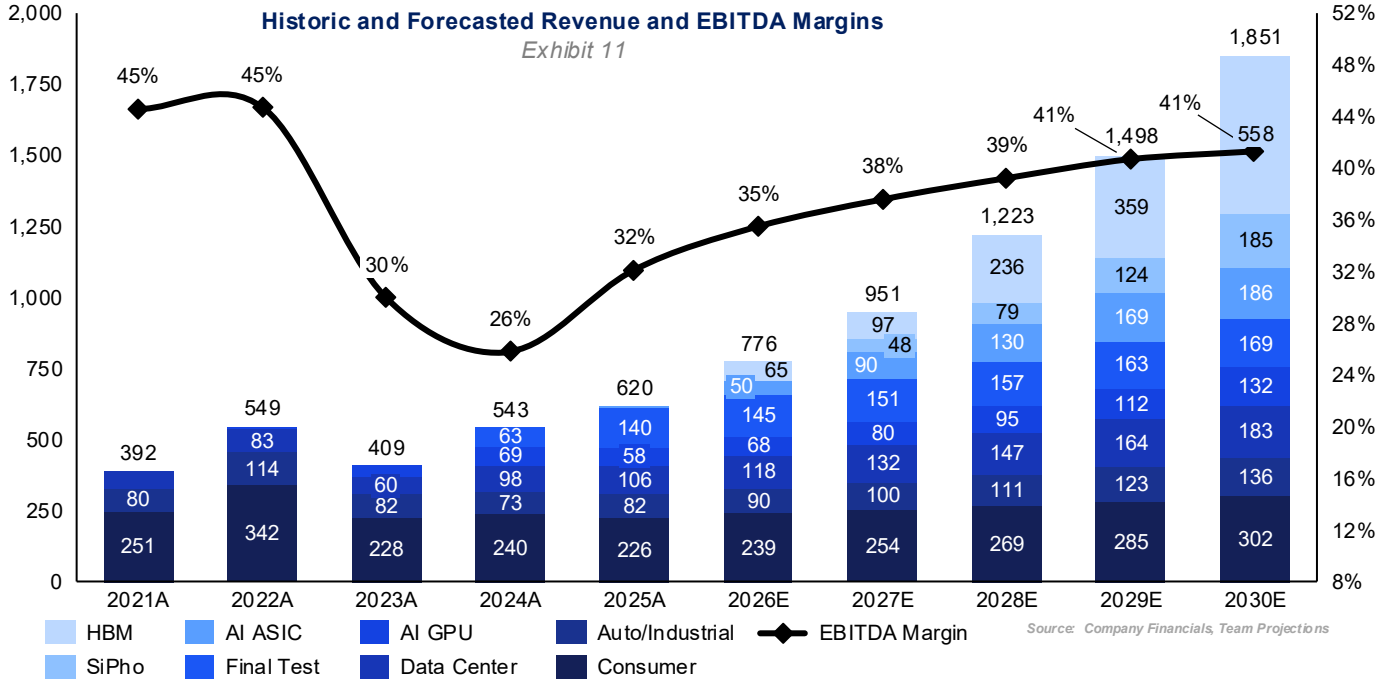


Source: AMD

Segment-Level TAM Forecasts



We believe the stock embeds an HBM outcome that is fundamentally inconsistent with how the memory industry works, how qualification actually happens, and where the company sits competitively. The bull case is easy to articulate: HBM demand is surging, test intensity is rising, and probe cards should see structurally higher content. While we agree on the industry backdrop aspect, our disagreement lies in TPRO's *position* within that backdrop. **Investors have extrapolated the momentum of the entire HBM ecosystem onto a company with minimal memory exposure, unclear qualification status, no incumbency, and participation limited to a small subset of the total HBM test flow.** The valuation reflects what the market *wants* TPRO to become rather than what it is likely to be based on evidence.



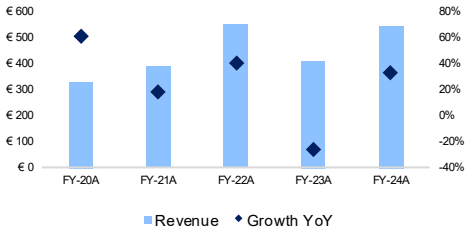
The first issue is that the accessible HBM opportunity for TPRO is far smaller than implied by the current share price. Although the 2027 HBM MEMS market is roughly €500–550m, most of that value sits in DRAM-side test steps tied to entrenched incumbents at **SK Hynix**, the dominant HBM producer. TPRO currently cannot access those stages, and its realistic participation is limited to logic base-die wafer probe and a narrow portion of early stack-level testing, which represent only a minority of total HBM probe spending. When sizing only the parts of the flow that TPRO can credibly win, we forecast €96.7m of HBM revenue in 2027. Consensus is near €250m. **The ~€150m gap between our view and the Street is not a forecasting nuance; it is a structural limit imposed by the parts of the HBM flow that are actually contestable. The Street's numbers implicitly assume TPRO can monetize a large share of the total HBM market, which is not realistic given its insertion points.**

Secondly, we believe the market is misreading competitive and qualification dynamics. The Street is effectively assuming a clean opening for a "third" HBM supplier, but **memory probe is the most relationship-anchored part of semiconductor test.** Qualification cycles span multiple product generations, engineering interfaces are tightly integrated into customer debug teams, and the risk tolerance around HBM, given its stack cost, is extremely low. TPRO is suspected to have qualified with only one memory manufacturer, but the company has not disclosed which one and has not confirmed whether shipments have begun. This is not the profile of a company about to scale across multiple HBM programs. Meanwhile, incumbents already ship HBM probe cards and remain embedded in customer roadmaps. Because **Samsung Electronics** is not the bottleneck in global HBM supply and because dual-sourcing is mandatory, **even a generous assumption of winning 70% of Samsung's accessible demand does not yield the revenue scale consensus models assume.** Management's own comments reinforce this: they described their HBM investments as **"investing blindly"**, and Investor Relations stated that HBM share will be **"hard to win"**. These remarks are incompatible with the high-confidence, multi-customer ramp implied by the valuation.

Third, the economics do not support the valuation. Early-cycle HBM probe ramps are margin-dilutive due to scrap, thermal-stress failures, debug loops and elevated engineering overhead. Yet consensus embeds margin levels similar to TPRO's mature logic business. These high margins are unlikely to be achieved upfront, as reiterated by investor relations. The mismatch becomes more severe when factoring in TPRO's decision to double capacity despite acknowledging that its core logic segment cannot fill the expanded footprint. The valuation thus assumes that HBM volumes will provide the necessary utilization to support returns. Our numbers show the opposite: **the accessible revenue simply does not exist at the scale required to justify the investment.** The reverse-DCF makes this even clearer, the stock price requires long-term HBM revenue, share and margin levels that would require TPRO to displace incumbents, win multiple memory nodes and run at high utilization across a newly expanded network. Nothing in the company's customer exposure, qualification progress or internal visibility supports that path.

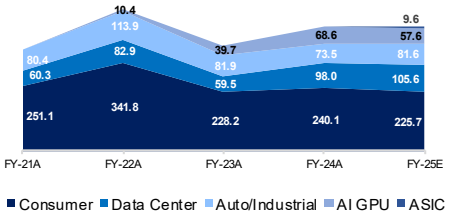
Finally, investors are valuing what TPRO *could be* in a best-case scenario rather than what it is most likely to be given industry structure. With little international coverage, low float outside Italy and a simple narrative link between "HBM growth" and "TPRO upside," the stock has become a story trade rather than a fundamentals-anchored one. Even as the broader semiconductor complex has flattened, including leaders such as **Nvidia**, TPRO has continued rising. We believe this divergence reflects sentiment rather than fundamentals. The company has no operating history in memory probe, no demonstrated traction, limited qualification visibility and a margin profile that is more likely to deteriorate, not expand, as HBM ramps.**In our view, TPRO is priced for a multi-year, high-share, high-margin HBM future that is neither visible to management, nor supported by customer relationships, nor aligned with how memory-test ecosystems evolve. The actual opportunity is smaller, slower and more margin-dilutive than the market assumes. As expectations converge with reality, we see meaningful downside.**

Revenue Trajectory – *Exhibit 12*



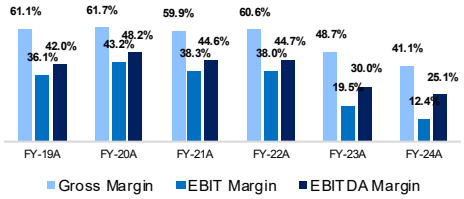
Source: Company Financials

Revenue per Subsegment – Advanced Logic – *Exhibit 13*



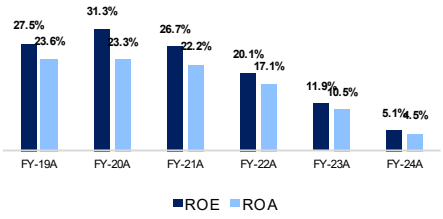
Source: Company Financials

Margin Trajectory– *Exhibit 14*



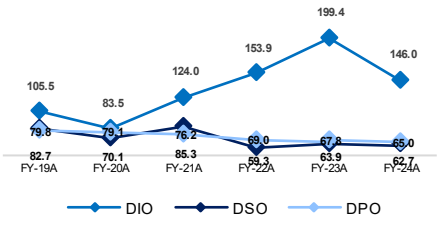
Source: Company Financials

Historical ROE & ROA– *Exhibit 15*



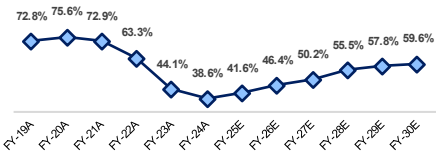
Source: Company Financials, Team Estimates

Operating Ratios – *Exhibit 16*



Source: Company Financials, Team Estimates

Asset Turnover Ratio – *Exhibit 17*



Source: Company Financials, Team Estimates

FINANCIAL ANALYSIS
Historical perspective

REVENUES
Revenue growth over the past 5 years has been volatile, with year-over-year figures reaching as high as 61% and dropping to as low at -25% in the downcycle during FY-23. On a segment level, the core Advance Logic business is mainly made up of Consumer, although this segment shrank in size between 2021 and today, while Auto & Industrial stayed flat, Data Center and AI rose, and ASIC is expected to ramp significantly in coming years.

The recent acquisitions of TPRO mask the lack of organic growth during the last fiscal year. For example, in the Q2-25 year-on-year revenue growth of 21.1% would be -7.8% ex-acquisitions.

MARGINS
Gross, Operating, and EBITDA margins have all compressed over the trailing 5-year period as TPRO has consolidated margin dilutive businesses. Post-consolidation, however, the margins turned around, with mgmt. currently guiding to 38-40% EBITDA margins by FY-27, a 13-15pp improvement vs. FY-24. Consensus expectations on margin improvements also include final testing becoming de-commoditized and complexity tailwinds.

RETURNS
Once again, as a result of the acquisitions, **both Return on Equity and Return on Assets has deteriorated over the period from FY-19 to FY-24.** However, given cost efficiencies between the subsegments of TPRO as well as operating leverage effects, these metrics should all improve in the forecast period, converging to historical averages.

CASH FLOWS & OPERATING EFFICIENCY
While some of TPRO's acquisitions dragged cash flows in the recent years, the company has operated with **stable and growing cash flows and a strong balance sheet with no debt.** The Operating Cycle has increased by 20 days between FY-19 and FY-24 due to Days Inventory Outstanding increasing by 40 days and Days Sales Outstanding falling only by 20 days.

Days Payable Outstanding decreased by approximately 15 days over the same period, meaning TPRO pays its accounts earlier on average. Additionally, the Cash Conversion Cycle of TPRO increased by ~35 days. Our model forecasts a slight improvement in the Cash Conversion Cycle between FY-25E and FY-30E. The annual CapEx spend as a % of Revenues is relatively normal for a technology business at 15%, and was forecasted as such, assuming no significant shifts in CapEx intensity in the forecast period.

Asset Turnover has also deteriorated, but due to increased efficiencies across the vertical segments of TPRO, we expect it to improve to close to 60% from lows of 38.6% in FY-24.

OVERALL FINANCIAL ASSESSMENT
The recent financial performance of TPRO reflects acquisition led growth rather than organic expansion. However, capacity expansion ahead can lead to significant organic growth in the core business, and a successful entry in the HBM market would provide further tailwinds to top-line through TAM expansion.

On the other hand, the timing of a successful entry should be dragged out due to existing relationships and dual sourcing, as well as a potential downturn in the HBM market when shortages fade.

We also view the target margins on this segment in the early years as inferior to that of the core business (albeit superior to final testing), and the total revenue opportunity to be below that of market expectations implied by our reverse DCF (€96.7mn vs. implied consensus of €150-300mn by FY-27).

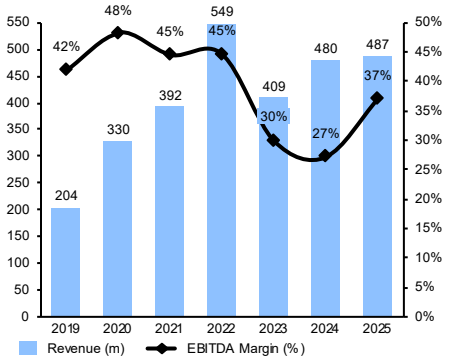
FINANCIAL FORECAST

METHODOLOGY
For the DCF analysis, we evaluated the performance of the firm, we broke down the company into four segments: **[1] Advanced Logic MEMS**, which is the legacy core of the business that includes the sub-segments of Consumer (mobile & PC), Auto/Industrial, Data Center, AI GPU, and the emerging AI ASICs segment; **[2] High Bandwidth Memory (HBM) MEMS**, **[3] Silicon Photonics (SiPho) Testing**, and **[4] Final Test**. We then conducted a comprehensive analysis, taking into account the end market growth rate, TPRO market share, and margin potential, to determine how collectively TPRO's different business segments drive value creation.

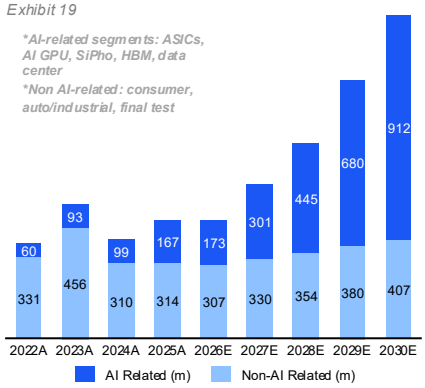
A top-down analysis is selected for 2 reasons. First, the company is highly demand driven by, and thus correlated with, the broader industry cycles within the logic chips. Capacity constraints has historically not been the major limitation as TPRO ensures spare capacity to meet ensuing demand. Second, there is limited ASP and volume data on individual probe cards, combined with the significant customizability of individual probe cards, casts doubt on the accuracy and feasibility of unit economics methods.

FINANCIAL FORECAST

Historic Advanced Logic Revenues - *Exhibit 18*



TPRO AI vs non-AI End Segment Revenues - *Exhibit 19*



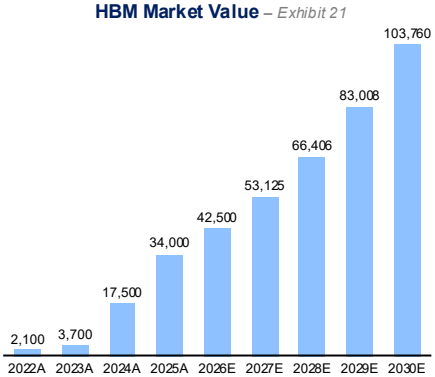
Source: Company disclosures, team estimates

Hyperscaler custom ASIC roadmap – *Exhibit 20*

Hyperscaler	Chip name	Year	Node
Google	TPU v6e (Trillium)	2024	4nm
	TPU v6p (Ironwood/Hammer)	2025	3nm
	TPU v7p (Hellcat)	2026E	3nm
	TPU v7e (Ibichi)	2026E	3nm
	TPU v8p	2028E	2nm
	TPU v8e	2028E	2nm
Amazon	Inferentia v 2.5	2024	5nm
	Trainium v 2 (Cayman)	2024	5nm
	Trainium v 2 R1 (Milano)	2025	5nm
	Trainium v 2 Ultra (R2, Milano)	2025	5nm
	Trainium v 3 (Mariana)	2026E	3nm
	Trainium v 4 (Maverick)	2028E	2nm
Microsoft	Maia 100 (Athena)	2024	5nm
	Maia 200 (Braga/Normandy)	2025	3nm
	Maia 300 (Griffin)	2026E	3nm
	Maiai 400	2027E	2nm
Meta	MTIA 1 (Artemis)	2024	5nm
	MTIA 1 (Athena)	2025	5nm
	MTIA 1.5 (Iris)	2026E	3nm
	MTIA 1.5 (Arke)	2027E	2nm
	MTIA 2 (Olympus)	2027E	2nm
	MTIA 3 (Ethna)	2028E	1.6nm

Source: Google, Amazon, Microsoft, Meta

HBM Market Value – *Exhibit 21*



Source: Bloomberg, averaged industry estimates

Advanced Logic MEMS Segment

REVENUES

Advanced Logic MEMS has been the core growth engine since TPRO's IPO in 2019. Revenue has increased from €204m in 2019 to €487m in 2025 (Q1-3 annualized). While CAGR has reached 15.57% through the years, growth has not been stable: the 22-23 downcycle led to fall of revenues by 140m (-26%), which still has recovered until today. Looking forward, we forecast top-line revenue based on end market sub-segment growth.

MARGINS

Margins hover at 42-45%, an industry leading figure as TPRO sits in the premium probe card market. However, TPRO exhibited margin contraction during the 22-23 industry downturn due operating leverage from fixed maintenance, workforce, and R&D costs, reaching a low of 27% in 2024. Advanced Logic MEMS margins across different end market sub-segments are similar. Management expressed confidence in returning to 40% margins in 2027, which is incorporated into the forecast.

SUB-SEGMENT 1: CONSUMER

The consumer segment comprises testing for chips in smartphones, PCs and home appliances. It historically was a strong contributor for TPRO at 50-60% of revenues, though this has decreased as other segments ramped. End market chips include SoCs, connectivity, and mixed-signal companion ICs. End-demand is tied to device cycles, so product cycles are shorter and pricing is typically more competitive. Looking forward, probe-card content is supported by continued node migration in leading consumer compute (e.g., next-gen flagship mobile and PC CPUs at 2nm-class) and increasing test complexity, e.g. chiplet architecture, which drive uptick in ASPs. TPRO stands to benefit as a tester for Apple and Intel chips. While mobile and PC are relatively saturated, SoC in home appliances are on the rise. We estimate a ~6% CAGR through 2030.

SUB-SEGMENT 2: AUTO/INDUSTRIAL

The auto/industrial segment include testing for chips used in automotive (powertrain/ADAS) and industrial applications (automation, power management, factory equipment). It is a smaller contributor for TPRO, with revenue fluctuating around the €80m to €110m range. The mix includes MCUs, power/analog and sensor-adjacent devices. Looking forward, probe-card content is supported by increases in semiconductor content per vehicle (ADAS compute, electrification and connectivity) and ongoing automation/energy-efficiency capex in industrial markets. Overall, we view the category as structurally growing at a ~10.7% CAGR.

SUB-SEGMENT 3: Data Center

The datacenter segment comprises non-accelerator chips used in cloud and enterprise infrastructure, including server CPUs, DPUs/SmartNICs, and connectivity silicon. Demand has been explosive, driven by the hyperscaler and OEM capex cycle. Looking forward, probe-card content should be driven along end market growth in data center related chips infrastructure. We estimate growth at 11.6% through 2030, as TPRO increases business exposure to AI.

SUB-SEGMENT 4: AI GPU

The AI GPU segment comprises accelerator chips used for AI training and inference (primarily GPUs deployed in hyperscale and enterprise datacenters). For Technoprobe, this is a high-value test end-market given extreme I/O density and bandwidth requirements, tight signal integrity constraints, and increasingly complex chip architectures. Looking forward, demand is driven by ongoing capacity build-out for AI infrastructure. New chip iterations create step-ups in test requirements as I/O counts and speeds scale. We estimate ~18% CAGR through 2030.

SUB-SEGMENT 5: ASIC

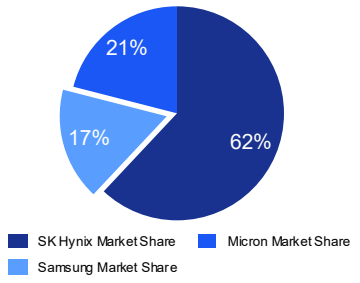
Application Specific Integrated Circuits (ASICs) are hyperscaler-designed AI accelerators for training and/or inference (e.g., Google, Amazon, Microsoft, Meta). ASICs operate at ultra-low voltages (~0.7–0.8V) with very high current draw (~600–1,000A), tightening SI/PI constraints and raising performance requirements for probe cards. Initial ASIC probe card production are to ramp in 2026 as TPRO announces probe card qualification progress. We estimate segment revenue scaling to €50m (2026E), €90m (2027E), and €130m (2028E).

HBM / DRAM MEMS Segment

DECOMMODIFYING THE MEMORY MARKET

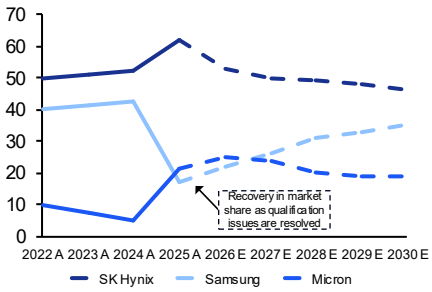
The High Bandwidth Memory (HBM) market is a significant new opportunity that Technoprobe is expanding into. The market is recent but has since expanded rapidly, from €2.1bn (2022) to €34bn (2025). Taking an average of industry projections, we estimate the market to continue growing at a CAGR of 25% through 2030. Importantly, HBM contributes to the de-commodification of memory testing. While conventional DRAM/NAND probing has historically been more standardized and low-margin, HBM test demands far higher I/O density, tighter signal integrity constraints, more demanding thermal/power conditions, and stricter known-good-die (KGD) requirements. The complexity also increases as the industry moves from HBM3/HBM3E today to HBM4/HBM4e ramping into production in 2026-27, and HBM5 later in the 2030. These factors raise probe-card performance requirements and creates attractive margins for Technoprobe, high-end probe manufacturer to enter. The HBM test market is estimated at ~1% of the broader HBM market.

Current HBM Market Share (%) – *Exhibit 22*



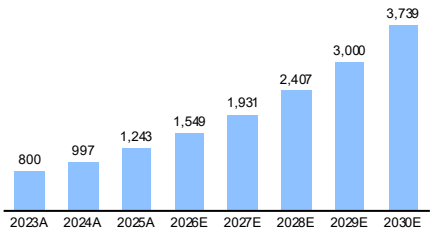
Source: Reuters

Forecasted HBM Market Share (%) – *Exhibit 23*



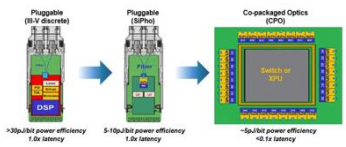
Source: Reuters, team estimates

Forecasted PIC Market Value (%) – *Exhibit 24*



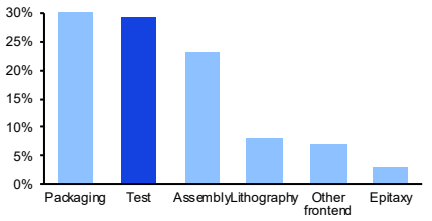
Source: Lightcounting

Evolution of Silicon Photonics – *Exhibit 25*



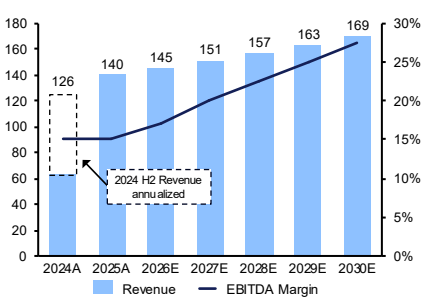
Source: TSMC 2025 Tech Symposium

PIC Cost Breakdown by Process (%) – *Exhibit 26a*



Source: Politecnico Milano

PIC Cost Breakdown by Process (%) – *Exhibit 26b*



Source: Company historic, team projections

BREAKING INTO THE OLIGOPOLY

The High Bandwidth Memory (HBM) market is an oligopoly, led by SK Hynix (~62%), followed by Micron (~21%) and Samsung (~17%). Historically, Samsung held a meaningfully higher share (~40%), but HBM qualification and ramp issues delayed production and drove share losses to peers.

Breaking into HBM therefore requires Technoprobe to secure a qualification at one of the three players. The company thus far only secured qualification with Samsung. FormFactor remains the entrenched incumbent across the oligopoly; at SK Hynix, FORM controls ~90% of HBM probing following joint development work, a position that is structurally difficult to dislodge. At SK Hynix, Formfactor and Micronics Japan have both secured qualification. Given high switching costs and long qualification cycles, we see limited opportunity for Technoprobe to penetrate other players in the near term.

Our base case follows that Technoprobe reaches a ~70% share at Samsung, alongside a recovery in Samsung's HBM share as qualification constraints normalize (~35% long-run share). Longer term, we expect the industry to trend gradually toward dual sourcing as volumes scale and product transitions progress from HBM4 to HBM4e and HBM5, which supports TPRO penetration into SK Hynix and Micron from 2028 onward.

Silicon Photonics Test Segment

BREAKING THROUGH THE "I/O" WALL

There exists a rising divergence between the speed at which data is processed and the speed at which data can be sent to other devices in traditional copper-based interconnects, known as the "I/O wall", which results in GPUs being idle 40-80% of the time. SiPho revolutionizes this by introducing data transmission via photons using modulated light, driving 5x data rates, 10x lower latency, and 8x lower power. The latest Photonics IC (PIC) iteration, Co-packaged Optics (CPO), relies on wafer-scale fabrication processes. As PIC wafer volumes continue to ramp, a scalable and complex test solution is needed, and the industry is demanding the standardized architecture of ATE, probers, handlers, and probe cards.

THE SiPho OPPORTUNITY

The PIC Market is current €1.2bn is expected to grow at a CAGR of 24.6% through 2030. Our team estimates the PIC test market at 12% of the PIC market, i.e. €205m in 2025. At the 2025 SWTest Conference, TPRO presented its first SiPho wafer probe card in collaboration with Marvell (MRVL), demonstrating solid R&D progress.

While competitors FormFactor and Jenoptik have also worked to development high-end SiPho probe cards, we believe that TPRO will gain an edge in the technology due to its ability to maintain higher-speed and higher-frequency testing (up to 67Ghz) with minimal signal loss.

As TPRO approaches qualification and PICs transition from pluggable optics to CPOs, our team estimates a market share entry at 20% in 2027, gradually increasing to 30% in 2030. EBITDA Margins are estimated at 25% in 2027, normalizing at 42% as production yields improve, in line with other high-end probe segments at TPRO.

Final Test Segment

FINAL TEST

Technoprobe entered Final Test segment in H2 FY24 via the €100m acquisition of DIS, and is positioned as the #1 global supplier of test interface boards (ex burn-in) with an 18% share. Final test refers to package-level electrical test (post-assembly/post-advanced packaging). Management discloses DIS standalone revenues at ~ €140m in 2025, with EBITDA margin at 12–15%.

While DIS remains margin dilutive in the near term, this segment provides a dual potential upside. Firstly, AI/HPC chip complexity will increasingly demand complex final testing solutions, which can carve out a unique high-end niche for TPRO.

Secondly, DIS adds vertical integration across the testing suppy chain for TPRO. This allows the company to provide full test-ecosystems in the future, opposed to the segregating test probe providers today. We forecast DIS revenue to stay flat at 4% CAGR, with a gradual EBITDA margin step up to 27.5% in 2030.

VALUATION

The target price of €11.7 is the result of a three stage DCF model considering a terminal growth rate of 2%, implying a 25.0% downside from the current price of €15.6. We think this is the best estimate we can provide of the value of the company, since it takes into account: 1) a long explicit forecasting period in which the company's margin and revenue growth story takes shape across different segments, 2) the downside to consensus estimates as competition ramps and new markets become more competitive ; 3) a fading phase in which the company will revert its returns to the mean; 4) the terminal growth period reflecting our view that TPRO's business will remain profitable and grow in-line with GDP.

Considering the stock's 160% run over the past 6-months and ~21% return YTD, we believe investors are overly optimistic about the growth prospects in new segments while not discounting execution risk, margin concerns, and commoditization. The current P/E multiple premium to its major peer FORM is at ~34%, which reflects the superior business model and profitability of TPRO. However, we believe this gap should shrink as TPRO enters segments that are less profitable, while FORM expands its business horizontally, protecting it from potential shifts in customer preferences and allowing it to offer a diverse set of solutions at the wafer level.

Details of our cost of capital calculations

In our analysis, we use a risk-free rate as the US 10y Treasury Yield (4.24%), and since the company has no debt on its balance sheet, we can disregard the cost of debt (although this has been added to the model for future reference, if mgmt. does decide to take on leverage).

To calculate the cost of equity, we use the classic formula from the CAPM Model given by: $r_E = r_f + \beta \times (E(r_m) - r_f)$. For the Equity Risk Premium, we use the Italian ERP taken from Damodaran Country Default Spreads and Risk Premiums library (6.69%). The beta of the stock vs. the FTSE MIB index has been calculated based on a 3-year regression and then adjusted with the Blume Adjustment, based on the observation that extreme betas (both high and low) tend to revert toward the average over time. The formula for the adjustment is: $Adj.\beta = 2/3 \times Raw\ \beta + 1/3 \times 1 = 2/3 \times 0.86 + 1/3 \times 1 = 0.91$. **The sensitivity analysis shows the asymmetric return profile of the investment,** with significant downside at lower perpetual growth rates and only moderate upside with high growth rates and lower WACC values.

Margins & Cash Flows

Gross Margins: We expect Gross Margins to increase to 59.4% by FY-30 as the Cost of Revenue decreases as a % of Revenues. This is a trend we see playing out as TPRO automates some of its testing, improves efficiency, and realizes synergies across its vertically integrated entities. **Operating Margins:** While operating margins have suffered and have gone as low as 12.4% in FY-24, we believe that SG&A declining as a % of Revenues will provide a larger uplift than the drag from R&D intensity which we modelled to increase as TPRO enters new markets and ramps up technological advancements. Overall, our target FY-27 Operating Margin of 26.3% reflects the view that Final Testing margins are inherently capped, and HBM will take longer to improve margins. The sell-side expects a margin improvement far above our estimates at 31.4%. This would require strong performance in HBM without excessive costs of acquiring customer relationships and taking market share, as well as a lack of margin drag from the DRAM segment, which Investor Relations has told us the company is also planning to penetrate. On the other hand, margins in the core business were assumed to not be at risk, and final testing to improve to 20% EBITDA margins by FY-27. **Overall, we consider our assumptions to be optimistic, and we believe the stock is currently priced for perfection with little margin for error on the margin as well as the revenue side, despite the significant tailwinds clearly visible in the market. Cash Flows:** Our model expects FCFO to ramp €118.3mn by FY-27 vs. sell-side consensus at €175.0mn. Our estimates reflect relatively high CapEx intensity as the upcoming two years will require spending on capacity expansion. It is important to mention that the capacity expansion has not yet started according to Investor Relations, and therefore most of the spend should come through in FY-26 and FY-27, dragging on cash flows.

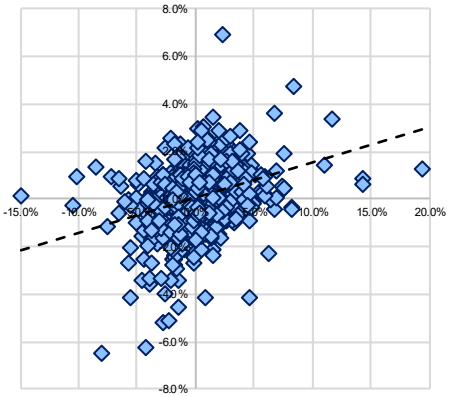
To validate our result in a relative terms, we run a multiple analysis on TPRO. **Peer group** – we consider a group of peer companies in the semiconductor space, including FormFactor, TPRO's closest peer, Advantest and Teradyne from the ATE space, closely integrated with the company, TSMC, TPRO's largest customer, Intel, ASML, as well as SK Hynix, to reflect the memory opportunity which TPRO is looking to address. We arrived at two implied valuations: one using the average of the peer group across EV/Sales, EV/EBITDA, and P/E multiples, as well as one using only FormFactor, as it is the company that most closely resembles TPRO's business model. Using these traditional multiples, we immediately see that TPRO is valued at a significant premium to peers both in terms of the average and the median multiple of the peer group. **The implied valuation based on the full peer group yields a 14.7% downside to the current price based on the EV/EBITDA FY-27 multiple,** which we find most appropriate as it reflects the end of the current guidance period, and includes TPRO's HBM expansion as well as margin normalization and capacity expansion. The downside based on FORM's EV/EBITDA multiple is lower at 4.8%, reflecting the market's belief that the valuation gap should normalize as EBITDA ramps with top-line expansion and margin growth. **From an operating perspective, we observe that TPRO's Cash Conversion Cycle and Operating Cycle are longer than both their major competitor FORM, as well as the peer group average.** Additionally, it takes TPRO 30+ days longer than FORM to convert Accounts Receivables into cash.

Bridge to Equity – *Exhibit 27*

Bridge to Equity	
PV of FCFO	**3,717.2**
% of EV	*52.7%*
Terminal Value	14,448.0
PV of TV	**3,336.7**
% of EV	*47.3%*
Enterprise Value	**7,053.9**
(-) Net Debt	656.83
EqV	**7,710.7**
Diluted ShO	651.76
Price/Share	€ 11.83
Current Price	€ 15.63
Upside/Downside	*-24.3%*

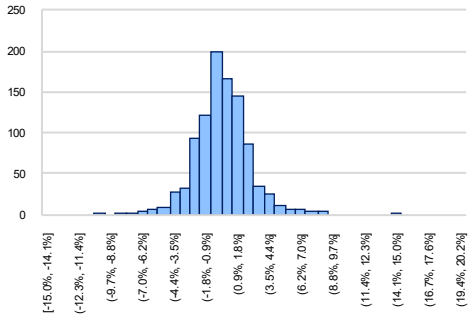
Source: Team Estimates

3y Beta Regression – TPRO vs. FTSE MIB – *Exhibit 28*



Source: Team Estimates

Distribution of Returns, TPRO vs. FTSE MIB – *Exhibit 29*



Source: Team Estimates

DCF Stage 1

In EUR Millions	2024 A	2025 E	2026 E	2027 E	2028 E	2029 E	2030 E
Revenues	**543.2**	**626.6**	**776.0**	**949.2**	**1,216.1**	**1,482.1**	**1,800.5**
% Growth	*32.7%*	*15.4%*	*23.8%*	*22.3%*	*28.1%*	*21.9%*	*21.5%*
EBITDA	**136.5**	**201.6**	**274.4**	**344.5**	**466.5**	**594.8**	**731.7**
% EBITDA Margin	*25.1%*	*32.2%*	*35.4%*	*36.3%*	*38.4%*	*40.1%*	*40.6%*
EBIT	**67.1**	**113.4**	**196.9**	**249.7**	**345.1**	**446.8**	**551.9**
% EBIT Margin	*12.4%*	*18.1%*	*25.4%*	*26.3%*	*28.4%*	*30.1%*	*30.7%*
(-) Taxes	34.2	27.2	47.3	59.9	82.8	107.2	132.5
Tax Rate	*35.3%*	*24.0%*	*24.0%*	*24.0%*	*24.0%*	*24.0%*	*24.0%*
NOPAT	**32.9**	**86.2**	**149.7**	**189.8**	**262.3**	**339.6**	**419.4**
% NOPAT Margin	*6.1%*	*13.8%*	*19.3%*	*20.0%*	*21.6%*	*22.9%*	*23.3%*
+ D&A	57.3	62.6	77.5	94.8	121.4	148.0	179.8
(-) Capex	(93.5)	(89.8)	(104.5)	(119.5)	(142.6)	(160.9)	(179.8)
% of Revenues	*(17.2%)*	*(14.3%)*	*(13.5%)*	*(12.6%)*	*(11.7%)*	*(10.9%)*	*(10.0%)*
(-) Change in NWC	(12.7)	13.9	(33.7)	(46.7)	(69.3)	(67.6)	(81.4)
% of Revenues	*(2.3%)*	*2.2%*	*(4.3%)*	*(4.9%)*	*(5.7%)*	*(4.6%)*	*(4.5%)*
FCFO	**(15.9)**	**72.9**	**89.0**	**118.3**	**171.8**	**259.1**	**338.0**
Year		0.09	1.09	2.09	3.09	4.09	5.09
Discount Factor		0.992	0.906	0.827	0.755	0.689	0.629
PV of FCFO		**72.3**	**80.6**	**97.9**	**129.7**	**178.5**	**212.7**

LT Growth Rate \ WACC	7.5%	8.5%	9.5%	10.5%	11.5%
3.0%	€ 19.36	€ 15.39	€ 12.67	€ 10.71	€ 9.24
2.5%	€ 18.17	€ 14.67	€ 12.22	€ 10.42	€ 9.04
2.0%	€ 17.19	€ 14.07	€ 11.83	€ 10.15	€ 8.86
1.5%	€ 16.37	€ 13.55	€ 11.49	€ 9.92	€ 8.69
1.0%	€ 15.67	€ 13.11	€ 11.19	€ 9.71	€ 8.54

LT Growth Rate \ WACC	7.5%	8.5%	9.5%	10.5%	11.5%
3.0%	*23.9%*	*-1.6%*	*-18.9%*	*-31.5%*	*-40.9%*
2.5%	*16.2%*	*-6.1%*	*-21.8%*	*-33.4%*	*-42.2%*
2.0%	*10.0%*	*-10.0%*	*-24.3%*	*-35.0%*	*-43.3%*
1.5%	*4.7%*	*-13.3%*	*-26.5%*	*-36.5%*	*-44.4%*
1.0%	*0.3%*	*-16.1%*	*-28.4%*	*-37.9%*	*-45.3%*

ESG

ESG factors are integral to Technophobe's long-term investment profile given its role in the semiconductor test ecosystem, where energy intensity, water availability, hazardous materials, skilled labour, and governance quality directly influence operating continuity, customer eligibility, and regulatory compliance. TPRO reports under CSRD/ESRS and has completed a Double Materiality assessment.

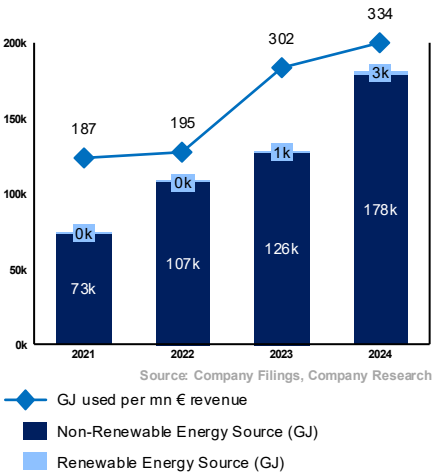
We believe the assessment of TPRO is best understood through the internal analytical framework outlined below, with broad market data incorporated for general context. According to the global market data provider Bloomberg, TPRO ranks in the 48.1st percentile of the global semiconductor peer group, ahead of its closest peer FormFactor at the 31.2nd percentile for total ESG score (Exhibit 30).

TPRO ESG Score Card – *Exhibit 30*

	Avg.	Enviro.	Social	Gov.
S&P Global	32	27	36	35
Bloomberg	48.1st pctl.	70.9th pctl.	N/A	N/A
Factset	27th pctl.	N/A	N/A	N/A
Morningstar	28.68 medium	N/A	N/A	N/A

Source: S&P Global, Bloomberg, FactSet, Morningstar

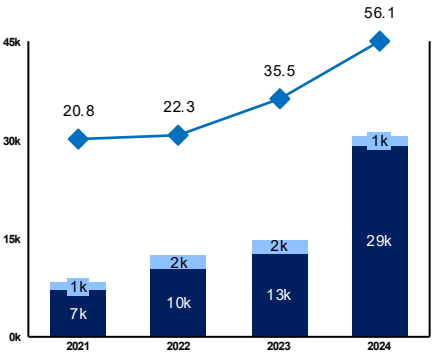
TPRO Energy Consumption Profile – *Exhibit 31*



Source: Company Filings, Company Research

GJ used per mn € revenue
Non-Renewable Energy Source (GJ)
Renewable Energy Source (GJ)

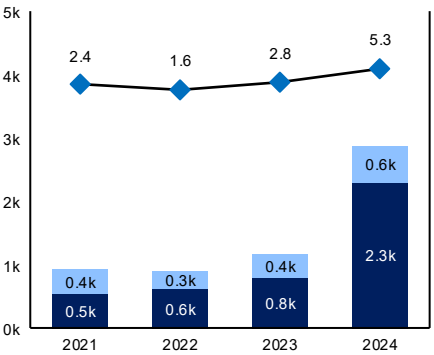
TPRO Carbon Emissions Profile – *Exhibit 32*



Source: Company Filings, Company Research

Tonnes of CO2e emitted per mn€ revenue
Scope 1 Emissions (tCO2e)
Scope 2 Emissions (tCO2e)

TPRO Waste Production Profile – *Exhibit 33*



Source: Company Filings, Company Research

Tonnes of waste produced per mn € revenue
Hazardous Waste (tonnes)
Non-Hazardous Waste (tonnes)

ENVIRONMENTAL

TPRO's environmental profile centres on a few material levers: energy use and GHG emissions, water management, and emerging regulation. These factors influence operating costs, production continuity, and customer procurement.

Energy: Energy consumption is the most material environmental factor for TPRO. As the company's test systems increase in complexity and performance requirements, manufacturing and testing processes demand higher and more stable electricity input, heightening exposure to power prices and overall energy-efficiency performance. Over the past four years, energy intensity, measured as gigajoules per million EUR of revenue, has increased in line with sector trends (Exhibit 31). Current mitigation measures centre on an energy-efficiency programme that includes process optimisation, facility upgrades, and behavioural initiatives. Onsite renewable generation has an installed capacity of 442 kWp, supplying less than 1.5% of total energy demand.

GHG Emissions: TPRO discloses Scope 1, Scope 2, and relevant Scope 3 emissions, as well as energy metrics, in alignment with ESRS E1. The company has not committed to science-based or net-zero-aligned targets and has not published a quantified decarbonisation pathway. In 2024, TPRO reported 56 tonnes CO_2e per million EUR of revenue (Exhibit 32). This is at the upper end of our proprietary range; comparable semiconductor manufacturing peers typically report approximately 34 to 59 tonnes CO_2e per million EUR of revenue. In our view, the absence of time-bound climate targets limits TPRO's ability to fully align with large customers' net-zero supply-chain expectations.

Water Management: Water availability is a material constraint in semiconductor production, but TPRO operates no production facilities in high-water-stress areas. In 2024, TPRO used 22,674 m³ of water, with only 103 m³ (0.45 percent) drawn from higher-risk regions.

Emerging Regulation: TPRO faces tightening environmental regulation across the semiconductor value chain. Hazardous substances are the primary current focus. The company monitors incoming materials and waste streams, manages hazardous substances in engineered areas, and uses authorised operators for disposal. Total hazardous and non-hazardous waste reached 2,871 tonnes, with a recycling or recovery rate of 16.3%, below typical sector practice (Exhibit 33). No material environmental incidents or fines were reported. In discussions with the CFO, the company indicated that it continues producing work-in-progress during demand downturns, accepting that some will become scrap.**The CFO described this as an intentional trade-off that preserves material availability and short lead times when demand recovers, structurally increasing waste intensity.**

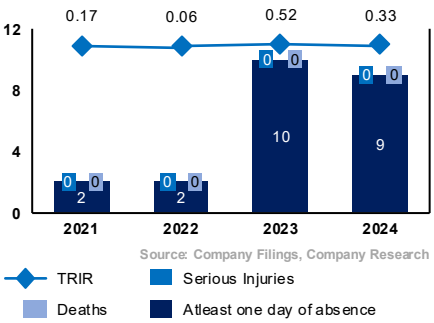
SOCIAL

TPRO operates in a high-skill, engineering-intensive segment where access to specialised talent is a core operational dependency. Material social factors centre on talent attraction and retention, workforce stability and availability, and health and safety performance. These factors directly shape execution quality, delivery reliability, and the company's ability to scale with customer demand. Strong workforce performance supports operational resilience; weak performance increases delivery and capacity risk.

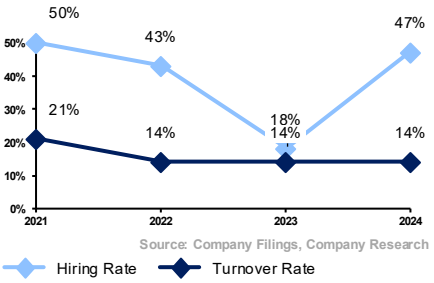
Health and Safety: TPRO has adopted an Occupational Health and Safety Management System (OHSMS) aligned with Article 30 of Legislative Decree no and ISO 45001. The OHSMS is supported by regular risk assessments, internal audits and the active involvement of worker safety representatives at each site. In 2024, TPRO recorded a Total Recordable Injury Rate (TRIR) of 0.33 per 200,000 hours vs the industry standard range of 0.5 to 0.7 (Exhibit 34).

Human Capital: TPRO reports a stable annual turnover rate of 14% and a hiring rate of 47.1% (Exhibit 35) . A 14% turnover rate aligns with typical levels in the semiconductor and technology sectors, where rates commonly fall in the low- to mid-teens. The elevated hiring rate indicates active workforce expansion, consistent with the company's reliance on specialised engineering talent. Combined, these metrics point to a growing but stable human-capital base, with no signs of abnormal attrition pressure. **This stability supports execution quality and delivery reliability in a high-skill, engineering-intensive operating model.**

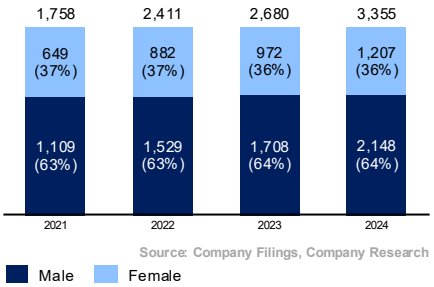
TPRO Workplace Safety Profile – *Exhibit 34*



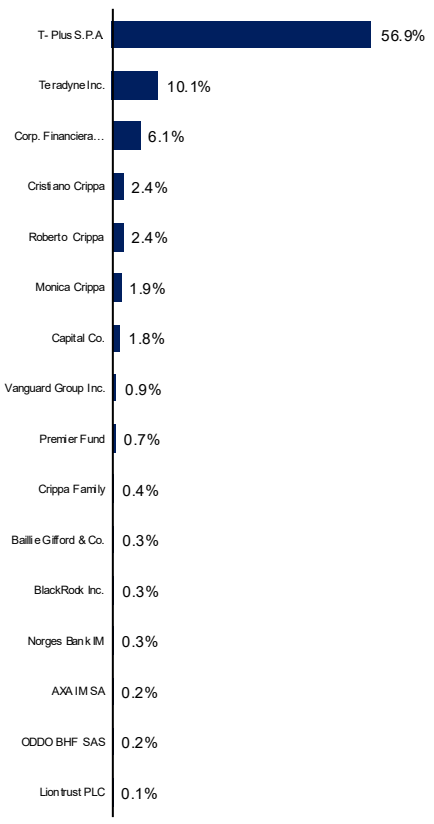
TPRO Hiring and Turnover Rate – *Exhibit 35*



TPRO Employee Demographics – *Exhibit 36*



TPRO Common Stock Ownership – *Exhibit 37*



Employee Diversity | TPRO employs 3,355 people across 10 countries. Disclosures cover gender and age distribution, role categories, training, turnover and selected pay-gap metrics, with some indicators still in ESRS phase-in. Women represent 36% of staff and make up 20% of senior executives, 29% of managers and 29% of the Board. Average training hours are 43 per employee and 64 for operators/technicians. The workforce is heavily unionised, with no reported disputes; 99.7% of EEA employees are covered by collective bargaining agreements.

GOVERNANCE

Leadership Structure: TPRO operates under a single-tier governance model with a 10-member Board of Directors, comprising three executive directors and seven non-executive directors, of which 56% are independent. The Board brings a mix of engineering, semiconductor-process, financial, and legal expertise. Board tenure ranges up to 25 years with an average of 6.33 years.

Shareholder Composition: Ownership is highly concentrated. T-PLUS SpA, the Crippa-family holding vehicle, controls 57% of share capital and 69% of voting rights, while individual Crippa family members own a further ~7% of common shares. This shareholder structure increases the importance of minority-protection mechanisms. Strategic investor Teradyne holds 10%, creating a dual-anchor setting that shapes technology alignment and related-party governance. The remaining free float is held by institutional and retail investors, with Spanish investment holding company Corporación Financiera Alba the largest at 6% (Exhibit 37).

Executive Compensation: Executive remuneration combines fixed pay with variable incentives linked to financial, operational and ESG KPIs. ESG-related indicators account for 10% of STI weighting, with the remainder driven primarily by turnover and EBITDA performance. Long-term incentives comprise a service-based Restricted Shares Plan and a Performance Shares Plan linked to financial metrics (Turnover growth and relative TSR) and a social ESG metric (Employee Engagement Index). No climate- or emissions-linked KPIs are embedded in LTIP design. **Relative to semiconductor-equipment peers, Technoprobe's incentive architecture remains less aligned with long-horizon sustainability and climate targets.**

INVESTMENT RISKS

Segment-Level risks include:

1) High-bandwidth memory (HBM): A risk to our sell recommendation is a better-than-expected entry into the HBM market by FY27 and in outer years. This risk would be materialized by a faster and higher capture of wallet share at memory players, and/or a wider adoption of vertical MEMS technologies in DRAM wafer-level testing, as opposed to mainly base logic-die and HBM-stack testing. **Mitigation:** Our DCF model already implies a successful penetration of the HBM market, with segment EBITDA margins at 36% in '26E (42% in '27E), and TPRO capturing 70% of Samsung testing share. An even more optimistic entry scenario would be hard to justify, and MEMS adoption at DRAM level is currently unnecessary given high parallelism.

2) Final testing. The final testing stage could be progressively un-commoditized due to increasingly complex packaging practices. Moreover, TPRO could leverage its DIS capabilities to cross sell wafer-level and final testing products. **Mitigation.** Similarly to HBM, our forecasting is aware of the above-mentioned trends (e.g., final testing reaching 27.5% EBITDA margin in '30E).

3) Advanced logic and AI. TPRO's main business segment, i.e., advanced logic testing, could benefit from increasing complexity given by tighter physical requirements, especially for AI products. **Mitigation.** The structural tailwind in advanced logic is already widely reflected in TPRO's share price. There is little to no room for upside surprise in this segment, while downside could be generated by less-than-perfect conversion of capacity doubling into sales or future order-book revisions at TSMC due to market cycles.

Company-level risks include:

1) Margin resilience. TPRO can benefit from operating leverage as sales increase, as well as potential EUR FX tailwinds inflating the top line. **Mitigation.** Analyzing trends through a bottom-up approach, we reach a 36.3% EBITDA margin in '27E, below management's guidance (38%).

2) Market structure. TPRO could gain additional share at TSMC given increasingly demanding testing requirements. Moreover, the memory market is an oligopoly of only three producers, so the certification process could be expedited. **Mitigation.** As discussed in the Investor Relations call with Dr. Di Terlizzi, wallet share at TSMC is expected to remain flat. In the HBM space, while TPRO is in talks with all three players, obtaining the certification remains a challenge, with FORM being an entrenched incumbent, and renewals likely needed with each new HBM generation.

MACRO RISKS

The **cylicality shift risk** refers to the risk of semiconductor-related industries moving from cyclical players to structural winners as AI becomes a structural driver of growth. **Mitigation.** The argument essentially takes a "this time is different" approach, which has repeatedly been proven dangerous. Moreover, our model does not assume a sharp correction to the current up-cycle, but rather a smoothing out of revenue growth, along with a reasonable stabilization of margins.

The **policy risk** includes the effect of re-shoring and other subsidies, which can keep AI-related CapEx elevated, indirectly supporting equipment investments and testing intensity. **Mitigation.** While the global AI race backdrop is a clear tailwind for TPRO, other aspects of the geopolitical climate can disproportionally hurt the company, i.e., any disruption in the China-Taiwan situation.

VALUATION RISKS

The **methodology risk** stems from the lower downside offered by our peer multiple analyses compared to our intrinsic DCF valuation. **Mitigation.** Our base case points to a significant (24.3%) gap, with sensitivity tables showing further widening should investors' WACC increase.

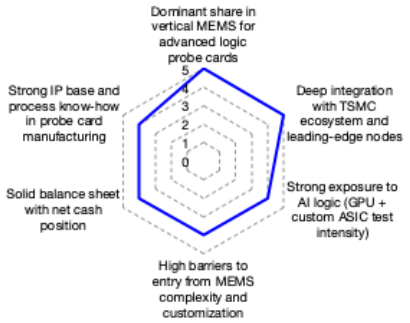
The **positioning risk** relates to some technical considerations for TPRO's stock. The free float is notably low due to high insider ownership, making the stock vulnerable to potential short squeezes. **Mitigation.** The stock also features sizeable institutional ownership, and can offer a compelling investing opportunity with multiples re-rating as the HBM narrative reverses.

APPENDIX

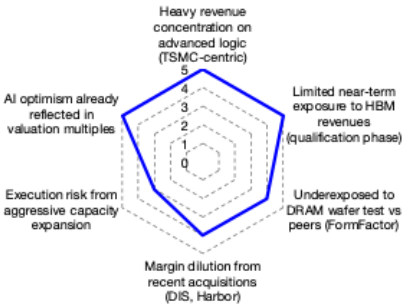
APPENDIX 1 – SWOT ANALYSIS

We implemented a SWOT analysis assigning to each driver a score between 1 (very low) and 5 (very high) considering strengths and weaknesses internal to Technoprobe, and the relative opportunities and threats coming from the market. The grade system used to analyse the overall position of FORM and the aspects considered for each category are summarized by the charts below.

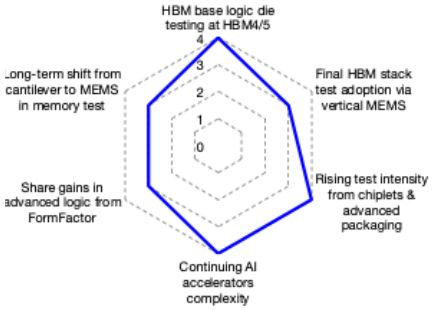
STRENGTHS	SCORE
Dominant share in vertical MEMS for advanced logic probe cards	5
Deep integration with TSMC ecosystem and leading-edge nodes	5
Strong exposure to AI logic (GPU + custom ASIC test intensity)	4
High barriers to entry from MEMS complexity and customization	4
Solid balance sheet with net cash position	4
Strong IP base and process know-how in probe card manufacturing	4
TOTAL	26



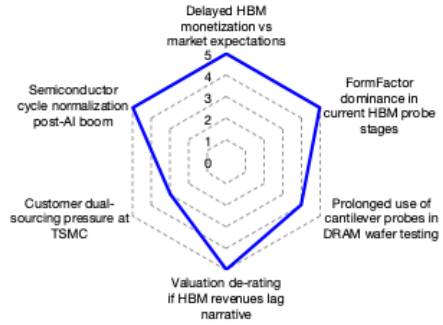
WEAKNESSES	SCORE
Heavy revenue concentration on advanced logic (TSMC-centric)	5
Limited near-term exposure to HBM revenues (qualification phase)	5
Underexposed to DRAM wafer test vs peers (FormFactor)	4
Margin dilution from recent acquisitions (DIS, Harbor)	4
Execution risk from aggressive capacity expansion	3
AI optimism already reflected in valuation multiples	5
TOTAL	26



OPPORTUNITIES	SCORE
HBM base logic die testing at HBM4/5	4
Final HBM stack test adoption via vertical MEMS	3
Rising test intensity from chiplets & advanced packaging	4
Continuing AI accelerators complexity	4
Share gains in advanced logic from FormFactor	3
Long-term shift from cantilever to MEMS in memory test	3
TOTAL	21



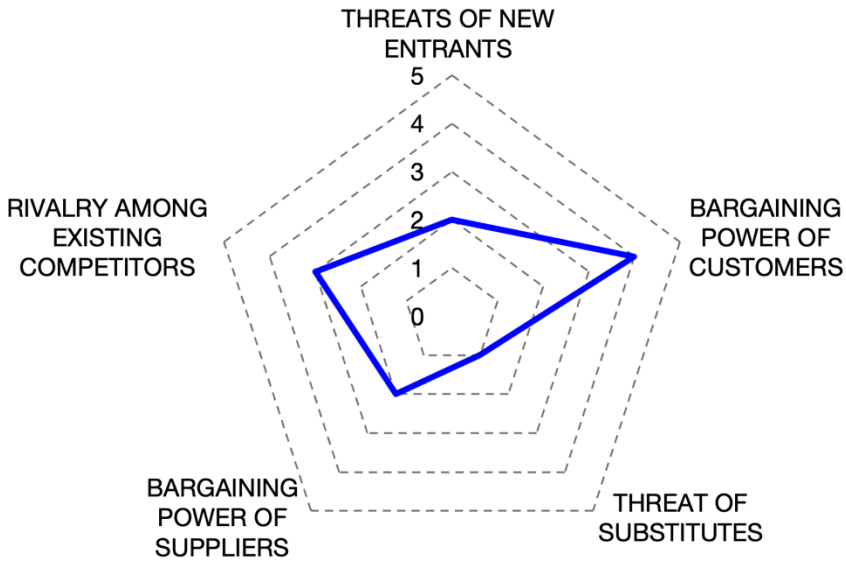
THREATS	SCORE
Delayed HBM monetization vs market expectations	5
FormFactor dominance in current HBM probe stages	5
Prolonged use of cantilever probes in DRAM wafer testing	4
Valuation de-rating if HBM revenues lag narrative	5
Customer dual-sourcing pressure at TSMC	3
Semiconductor cycle normalization post-AI boom	5
TOTAL	27



APPENDIX 2 – PORTER'S FIVE FORCES ANALYSIS

Legend

0 No threat
1 Very low
2 Low
3 Moderate
4 High
5 Very high



THREATS OF NEW ENTRANTS – LOW (2)

The threat of new entrants for TPRO is structurally low, especially in the advanced logic market. The reason is twofold:
a) there are very high technological barriers, with the development of vertical MEMS technologies requiring intense capital investments and years of research and development by highly qualified personnel;
b) there are stringent qualification cycles, with incumbents such as TPRO and FORM holding deep, entrenched, often customized partnerships with end clients as well as several key players along the value chain.

BARGAINING POWER OF CUSTOMERS – HIGH (4)

Sales are highly concentrated, with TSMC likely representing over 70% of revenues either directly or indirectly. This naturally forms high customer negotiating leverage, as reflected by the effects of TSMC-led dual sourcing requirements. Price pressure potential, however, is mitigated by considerable switching costs, materialized by qualification risks, yield sensitivity, and time-to-market constraints for TSMC.

THREAT OF SUBSTITUTES – VERY LOW (1)

There is virtually no threat of substitutes, as there is no alternative for probe cards in wafer-level testing. There is a choice between probe card technologies, e.g., between cantilever and vertical MEMS. The same reasoning is applicable to final testing, where TPRO operates through DIS.

BARGAINING POWER OF SUPPLIERS – LOW (2)

Suppliers present low to moderate bargaining power, as TPRO needs to respect short time-to-costomer cycles but some specialized inputs remain outsourced. However, TPRO has deeply mitigated this risk with vertical integration (e.g., with the Microfabrica acquisition) and with long-term relationships.

RIVALRY AMONG EXISTING COMPETITORS – MODERATE (3)

The advanced logic market has long been a duopoly, with TPRO and FORM competing in part for TSMC wallet share but largely benefiting from the lack of other contenders. However, as TPRO moves into HBM, the competition will intensify, with FORM and Asian competitors such as Micronics Japan Company already holding deep links with memory players.

APPENDIX 3 – INCOME STATEMENT

Units in millions of EUR
Technoprobe SpA (BIT: TPRO)

Fiscal Year	**2019**	**2020**	**2021**	**2022**	**2023**	**2024**	**2025**	**2026**	**2027**	**2028**	**2029**	**2030**
Calendar Date	12/31/19	12/31/20	12/31/21	12/31/22	12/31/23	12/31/24	12/31/25	12/31/26	12/31/27	12/31/28	12/31/29	12/31/30
Period Type	FY	FY	FY	FY	FY	FY	FY	FY	FY	FY	FY	FY
Fiscal Period	**FY-19A**	**FY-20A**	**FY-21A**	**FY-22A**	**FY-23A**	**FY-24A**	**FY-25E**	**FY-26E**	**FY-27E**	**FY-28E**	**FY-29E**	**FY-30E**
Income Statement												
Revenue	**204,4**	**329,5**	**391,7**	**548,9**	**409,3**	**543,2**	**626,6**	**776,0**	**949,2**	**1.216,1**	**1.482,1**	**1.800,5**
Growth YoY		*61,3%*	*18,9%*	*40,1%*	*-25,4%*	*32,7%*	*15,4%*	*23,8%*	*22,3%*	*28,1%*	*21,9%*	*21,5%*
(-) Cost of Revenue	(79,4)	(126,1)	(157,0)	(216,1)	(209,9)	(319,7)	(345,9)	(370,0)	(441,3)	(537,1)	(624,6)	(731,8)
Gross Profit	**124,9**	**203,4**	**234,7**	**332,8**	**199,3**	**223,4**	**280,6**	**406,0**	**507,8**	**679,0**	**857,5**	**1.068,7**
Gross Margin	*61,1%*	*61,7%*	*59,9%*	*60,6%*	*48,7%*	*41,1%*	*44,8%*	*52,3%*	*53,5%*	*55,8%*	*57,9%*	*59,4%*
(-) Research & Development	(14,0)	(20,6)	(33,7)	(56,4)	(56,8)	(63,4)	(60,0)	(80,1)	(104,9)	(143,4)	(185,7)	(252,1)
(-) Sales, General & Administrative	(36,9)	(40,4)	(51,4)	(67,7)	(62,8)	(92,9)	(107,1)	(129,0)	(153,2)	(190,5)	(225,0)	(264,7)
(-) Net Impairment of Financial Assets	(0,3)	(0,1)	0,2	(0,2)	0,0	(0,1)	–	–	–	–	–	–
EBIT	**73,7**	**142,4**	**149,9**	**208,4**	**79,8**	**67,1**	**113,4**	**196,9**	**249,7**	**345,1**	**446,8**	**551,9**
EBIT Margin	*36,1%*	*43,2%*	*38,3%*	*38,0%*	*19,5%*	*12,4%*	*18,1%*	*25,4%*	*26,3%*	*28,4%*	*30,1%*	*30,7%*
(+) Other Income (Expenses), Net	1,6	2,5	(4,5)	(4,2)	1,9	2,5	0,6	0,7	0,9	1,1	1,4	1,7
(+) Finance Income	1,4	0,2	0,1	1,2	8,6	17,1	6,5	8,1	9,9	12,6	15,4	18,7
(-) Finance Expenses	(0,1)	(0,3)	(0,2)	(0,2)	(0,3)	(1,6)	(0,6)	(0,8)	(1,0)	(1,2)	(1,5)	(1,8)
(+) Foreign Exchange Gains (Losses)	1,4	(8,1)	7,1	1,9	(4,8)	11,9	1,5	1,8	2,2	2,9	3,5	4,2
Pre-Tax Profit	**78,0**	**136,8**	**152,4**	**207,2**	**85,2**	**97,0**	**121,4**	**206,7**	**261,7**	**360,5**	**465,6**	**574,7**
(-) Income Tax Expense	(11,8)	(35,2)	(33,1)	(59,0)	12,1	(34,2)	(29,1)	(49,6)	(62,8)	(86,5)	(111,7)	(137,9)
Net Income	**66,1**	**101,6**	**119,3**	**148,2**	**97,4**	**62,8**	92,2	157,1	198,9	274,0	353,8	436,8
(-) Attributable to Non-Controlling Interests	–	–	(1,0)	0,3	0,4	(1,0)	(1,0)	(1,0)	(1,0)	(1,0)	(1,0)	(1,0)
Net Income to Parent	**66,1**	**101,6**	**120,4**	**147,9**	**97,0**	**63,8**	91,2	156,1	197,9	273,0	352,8	435,7
(/) Weighted Avg. No. of Ordinary Shares	500,0	500,8	576,0	597,9	600,3	630,7	630,7	630,7	630,7	630,7	630,7	630,7
Basic & Diluted EPS	**€0,13**	**€0,20**	**€0,21**	**€0,25**	**€0,16**	**€0,10**	**€0,14**	**€0,25**	**€0,31**	**€0,43**	**€0,56**	**€0,69**
(+) Net Impairment of Financial Assets	0,3	0,1	(0,2)	0,2	(0,0)	0,1	–	–	–	–	–	–
(+) Depreciation, Amortization & Impairment	11,8	16,5	25,0	36,7	42,9	69,3	88,2	77,5	94,8	121,4	148,0	179,8
EBITDA	**85,8**	**158,9**	**174,7**	**245,4**	**122,7**	**136,5**	**201,6**	**274,4**	**344,5**	**466,5**	**594,8**	**731,7**
EBITDA Margin	*42,0%*	*48,2%*	*44,6%*	*44,7%*	*30,0%*	*25,1%*	*32,2%*	*35,4%*	*36,3%*	*38,4%*	*40,1%*	*40,6%*
(+) Asia	101,2	149,6	182,4	356,9	178,8	254,6	293,6	363,7	444,8	569,9	694,6	843,8
% of Total	*49,5%*	*45,4%*	*46,6%*	*65,0%*	*43,7%*	*46,9%*	*46,9%*	*46,9%*	*46,9%*	*46,9%*	*46,9%*	*46,9%*
(+) Americas	38,1	132,6	33,0	153,4	187,9	250,3	288,7	357,5	437,3	560,3	682,8	829,6
% of Total	*18,7%*	*40,3%*	*8,4%*	*28,0%*	*45,9%*	*46,1%*	*46,1%*	*46,1%*	*46,1%*	*46,1%*	*46,1%*	*46,1%*
(+) Europe ex. Italy	56,2	36,5	166,7	28,7	31,6	26,6	30,7	38,1	46,6	59,7	72,7	88,3
% of Total	*27,5%*	*11,1%*	*42,6%*	*5,2%*	*7,7%*	*4,9%*	*4,9%*	*4,9%*	*4,9%*	*4,9%*	*4,9%*	*4,9%*
(+) Italy	8,8	10,7	9,6	9,8	10,9	11,7	13,5	16,7	20,5	26,2	31,9	38,8
% of Total	*4,3%*	*3,3%*	*2,5%*	*1,8%*	*2,7%*	*2,2%*	*2,2%*	*2,2%*	*2,2%*	*2,2%*	*2,2%*	*2,2%*
Revenue	**204,4**	**329,5**	**391,7**	**548,9**	**409,3**	**543,2**	**626,6**	**776,0**	**949,2**	**1.216,1**	**1.482,1**	**1.800,5**

APPENDIX 4 – BALANCE SHEET STATEMENT

Balance Sheet												
Assets												
Cash and Cash Equivalents	91,8	158,3	146,8	411,0	361,8	666,4	726,8	782,9	863,7	975,9	1.178,1	1.448,6
Inventories	23,0	34,8	71,9	110,4	119,0	136,8	135,5	141,9	169,3	206,0	239,6	280,7
Trade Receivables	46,3	80,3	102,8	75,4	67,8	118,8	114,5	150,3	183,8	235,6	287,1	348,8
Property, Plant & Equipment	102,0	136,3	179,0	220,1	277,7	338,9	366,1	393,1	417,9	439,0	451,9	451,9
Intangible Assets	6,9	6,0	6,7	10,7	17,9	65,5	75,6	93,6	114,5	146,7	178,8	217,3
Goodwill	9,8	9,0	9,8	10,4	25,5	43,7	43,7	43,7	43,7	43,7	43,7	43,7
Other Assets	10,7	20,3	30,2	39,2	84,1	82,0	89,4	110,7	135,4	173,4	211,4	256,8
Total Assets	**280,7**	**435,9**	**537,3**	**866,8**	**928,4**	**1.408,3**	**1.507,9**	**1.672,5**	**1.884,6**	**2.176,6**	**2.546,9**	**3.004,0**
Liabilities												
Trade Payables	17,4	27,3	32,8	40,9	39,0	56,9	65,3	73,8	88,0	107,1	124,6	146,0
Non-Current Lease Liabilities	2,0	1,8	5,5	5,8	10,4	13,8	13,8	13,8	13,8	13,8	13,8	13,8
Provision for Risks & Charges	2,0	2,0	11,6	20,1	20,1	21,6	21,6	21,6	21,6	21,6	21,6	21,6
Other Liabitilies	19,3	80,6	41,1	63,1	41,6	78,8	78,8	78,8	78,8	78,8	78,8	78,8
Total Liabilities	**40,7**	**111,7**	**91,1**	**129,8**	**111,1**	**171,1**	**179,5**	**188,0**	**202,2**	**221,4**	**238,8**	**260,2**
Equity												
Share Capital	5,0	5,8	5,8	6,0	6,0	6,5	6,5	6,5	6,5	6,5	6,5	6,5
Reserves	168,3	219,7	319,7	582,0	712,8	1.167,2	1.231,0	1.323,3	1.479,3	1.677,2	1.950,2	2.303,0
Retained Earnings	65,2	96,6	118,3	147,9	97,0	63,8	92,2	156,1	197,9	273,0	352,8	435,7
Total Equity to Parent	**238,5**	**322,0**	**443,8**	**735,9**	**815,8**	**1.237,6**	**1.329,8**	**1.485,9**	**1.683,8**	**1.956,7**	**2.309,5**	**2.745,2**
Equity to Non-Controlling Interests	1,6	2,2	2,5	1,0	1,5	(0,4)	(1,4)	(1,4)	(1,4)	(1,4)	(1,4)	(1,4)
Total Equity	**240,0**	**324,2**	**446,3**	**737,0**	**817,3**	**1.237,2**	**1.328,4**	**1.484,4**	**1.682,3**	**1.955,3**	**2.308,1**	**2.743,8**
Total Equity & Liabilities	**280,7**	**435,9**	**537,3**	**866,8**	**928,4**	**1.408,3**	**1.507,9**	**1.672,5**	**1.884,6**	**2.176,6**	**2.546,9**	**3.004,0**

APPENDIX 5 – CASH FLOW STATEMENT

Fiscal Period	FY-19A	FY-20A	FY-21A	FY-22A	FY-23A	FY-24A	FY-25E	FY-26E	FY-27E	FY-28E	FY-29E	FY-30E
Cash Flow Statement												
Pre-Tax Profit	**78,0**	**136,8**	**152,4**	**207,2**	**85,2**	**97,0**	**121,4**	**206,7**	**261,7**	**360,5**	**465,6**	**574,7**
Amortization Depreciation & Impairment	11,8	14,8	25,0	36,7	42,9	69,3	62,6	77,5	94,8	121,4	148,0	179,8
Gains (Losses) on Disposals	0,0	(0,2)	(0,2)	(0,2)	(0,1)	0,0	–	–	–	–	–	–
Net Finance (Income) Expenses	(1,2)	0,0	0,1	(1,0)	(8,3)	(15,5)	–	–	–	–	–	–
Provision to Funds	–	–	–	–	16,9	10,2	–	–	–	–	–	–
Other Non-Cash adjustments	7,1	2,2	13,7	16,9	(3,2)	(11,7)	–	–	–	–	–	–
Operating Cash Flow Before Changes in NWC	**95,6**	**153,6**	**191,1**	**259,6**	**133,4**	**149,4**	**183,9**	**284,2**	**356,5**	**481,9**	**613,5**	**754,4**
Changes in Inventories	(16,9)	(11,9)	(38,1)	(45,4)	(19,7)	0,9	1,2	(6,4)	(27,4)	(36,8)	(33,6)	(41,1)
Changes in Trade Receivables	(14,4)	(52,0)	(22,1)	27,3	11,7	(44,6)	4,3	(35,8)	(33,5)	(51,7)	(51,5)	(61,7)
Changes in Trade Payables	8,2	5,3	5,4	8,2	(3,5)	22,7	8,4	8,5	14,2	19,1	17,4	21,4
Changes in Other Assets/Liabilities	1,0	(4,0)	10,2	0,8	(11,5)	8,4	(7,4)	(21,3)	(24,7)	(38,1)	(37,9)	(45,4)
Uses for Risks & Charges/Employee Benefits	(1,1)	(1,4)	(1,7)	(5,3)	(4,0)	(4,6)	–	–	–	–	–	–
Income Taxes Paid	(3,2)	(13,2)	(63,4)	(37,9)	(44,6)	(7,8)	(29,1)	(49,6)	(62,8)	(86,5)	(111,7)	(137,9)
Operating Cash Flow	**69,2**	**76,4**	**81,3**	**207,2**	**61,8**	**124,4**	**161,3**	**179,6**	**222,3**	**288,0**	**396,2**	**489,7**
Net CapEx	(36,1)		(57,9)	(73,3)	(58,0)	(84,0)	(89,8)	(104,5)	(119,5)	(142,6)	(160,9)	(179,8)
Purchase of Intangible Assets	(0,6)		(1,0)	(5,1)	(1,1)	(9,4)	(10,1)	(18,0)	(20,9)	(32,2)	(32,1)	(38,4)
Net Divestiures/ (Investments) in Financial Assets	(0,9)		(0,1)	(0,1)	1,9	(1,3)	–	–	–	–	–	–
Acquistion of Subsidiaries, Net of Cash	(19,3)		–	–	(41,7)	(81,6)	–	–	–	–	–	–
Finance Income Received			–	0,2	5,4	7,6	–	–	–	–	–	–
Net Cash Flow from Investing Activities	**(56,9)**	**(50,6)**	**(59,0)**	**(78,3)**	**(93,4)**	**(168,8)**	(99,9)	(122,5)	(140,4)	(174,8)	(193,0)	(218,2)
Proceeds from Borrowings	–		–	–	–	0,0	–	–	–	–	–	–
Financial Liabilities Reimbursement	–		(30,4)	(4,6)	–	–	–	–	–	–	–	–
Change in Lease Liabilities	(0,5)		(2,5)	(3,1)	(3,0)	(3,3)	–	–	–	–	–	–
Finance Expenses Paid	(0,0)		(0,2)	(0,2)	(0,3)	(1,6)	–	–	–	–	–	–
Capital Increase	5,5		0,1	139,4	–	384,7	–	–	–	–	–	–
Acquistion of Treasury Shares			–	–	(11,7)	(34,7)	–	–	–	–	–	–
Acquistion of Minorities			–	–	–	–	–	–	–	–	–	–
Dividend Paid	(15,5)		(4,6)	(1,1)	–	(1,2)	–	–	–	–	–	–
NCI							(1,0)	(1,0)	(1,0)	(1,0)	(1,0)	(1,0)
Net Cash Flow from Financing Activities	**(10,4)**	**22,8**	**(37,6)**	**130,3**	**(15,0)**	**344,0**	(1,0)	(1,0)	(1,0)	(1,0)	(1,0)	(1,0)
Cash Flow Generated (Used) During Period	**1,9**	**70,2**	**(15,3)**	**259,2**	**(46,7)**	**299,6**	**60,4**	**56,1**	**80,8**	**112,2**	**202,2**	**270,5**
Cash & Cash Equivalents BoP	**89,4**	**91,8**	**158,3**	**146,7**	**411,0**	**361,8**	666,4	726,8	782,9	863,7	975,9	1.178,1
Changes in Cash & Cash Equivalents	1,9	70,2	(15,3)	259,2	(46,7)	299,6	60,4	56,1	80,8	112,2	202,2	270,5
Exchange Differnces	0,5	(3,7)	3,8	5,1	(2,5)	5,0	–	–	–	–	–	–
Cash & Cash Equivalents EoP	**91,8**	**158,3**	**146,7**	**411,0**	**361,8**	**666,4**	**726,8**	**782,9**	**863,7**	**975,9**	**1.178,1**	**1.448,6**

APPENDIX 6 – DRIVERS AND METRICS

IS Drivers												
COGS % of Revenue	*38,9%*	*38,3%*	*40,1%*	*39,4%*	*51,3%*	*58,9%*	*55,2%*	*47,7%*	*46,5%*	*44,2%*	*42,1%*	*40,6%*
R&D % of Revenue	*6,8%*	*6,2%*	*8,6%*	*10,3%*	*13,9%*	*11,7%*	*9,6%*	*10,3%*	*11,1%*	*11,8%*	*12,5%*	*14,0%*
SG&A % of Revenue	*18,1%*	*12,3%*	*13,1%*	*12,3%*	*15,3%*	*17,1%*	*17,1%*	*16,6%*	*16,1%*	*15,7%*	*15,2%*	*14,7%*
Net Impairment of Financial Assets % of Revenue	*0,1%*	*0,0%*	*-0,1%*	*0,0%*	*0,0%*	*0,0%*	*0,0%*	*0,0%*	*0,0%*	*0,0%*	*0,0%*	*0,0%*
Net Other Income % of Revenue	*0,8%*	*0,8%*	*-1,1%*	*-0,8%*	*0,5%*	*0,5%*	*0,1%*	*0,1%*	*0,1%*	*0,1%*	*0,1%*	*0,1%*
Finance Income	*0,7%*	*0,1%*	*0,0%*	*0,2%*	*2,1%*	*3,1%*	*1,0%*	*1,0%*	*1,0%*	*1,0%*	*1,0%*	*1,0%*
Finance Expenses	*-0,1%*	*-0,1%*	*-0,1%*	*0,0%*	*-0,1%*	*-0,3%*	*-0,1%*	*-0,1%*	*-0,1%*	*-0,1%*	*-0,1%*	*-0,1%*
Foreign Exchange Gains (Losses)	*0,7%*	*-2,4%*	*1,8%*	*0,3%*	*-1,2%*	*2,2%*	*0,2%*	*0,2%*	*0,2%*	*0,2%*	*0,2%*	*0,2%*
Tax Rate	*15,2%*	*25,7%*	*21,7%*	*28,5%*	*-14,2%*	*35,3%*	*24,0%*	*24,0%*	*24,0%*	*24,0%*	*24,0%*	*24,0%*
BS Drivers												
DIO	105,5	83,5	124,0	153,9	199,4	146,0	143,0	140,0	140,0	140,0	140,0	140,0
DSO	82,7	70,1	85,3	59,3	63,9	62,7	66,7	70,7	70,7	70,7	70,7	70,7
Intangible Assets % of Revenue	*3,4%*	*1,8%*	*1,7%*	*2,0%*	*4,4%*	*12,1%*	*12,1%*	*12,1%*	*12,1%*	*12,1%*	*12,1%*	*12,1%*
Other Assets % of Revenue	*5,2%*	*6,1%*	*7,7%*	*7,1%*	*20,6%*	*15,1%*	*14,3%*	*14,3%*	*14,3%*	*14,3%*	*14,3%*	*14,3%*
DPO	79,8	79,1	76,2	69,0	67,8	65,0	68,9	72,8	72,8	72,8	72,8	72,8
Capex							89,8	104,5	119,5	142,6	160,9	179,8
Depreciation							62,6	77,5	94,8	121,4	148,0	179,8
NWC	51,9	87,7	142,0	144,9	147,9	198,7	184,8	218,4	265,1	334,4	402,1	483,5
Change in NWC		35,8	54,3	3,0	2,9	50,8	(13,9)	33,7	46,7	69,3	67,6	81,4
Operating Cycle	188,2	153,7	209,3	213,2	263,3	208,7	209,7	210,7	210,7	210,7	210,7	210,7
Cash Conversion Cycle	108,5	74,6	133,1	144,2	195,5	143,8	140,8	137,9	137,9	137,9	137,9	137,9
CFS Drivers												
CapEx % of Revenue	*17,6%*	–	*14,8%*	*13,4%*	*14,2%*	*15,5%*	*14,3%*	*13,5%*	*12,6%*	*11,7%*	*10,9%*	*10,0%*
D&A % of Revenue	*5,8%*	*4,5%*	*6,4%*	*6,7%*	*10,5%*	*12,8%*	*10,0%*	*10,0%*	*10,0%*	*10,0%*	*10,0%*	*10,0%*
Return & Other Financial Metrics												
ROE	*27,5%*	*31,3%*	*26,7%*	*20,1%*	*11,9%*	*5,1%*	*6,9%*	*10,6%*	*11,8%*	*14,0%*	*15,3%*	*15,9%*
ROA	*23,6%*	*23,3%*	*22,2%*	*17,1%*	*10,5%*	*4,5%*	*6,1%*	*9,4%*	*10,6%*	*12,6%*	*13,9%*	*14,5%*
EPS	€0,13	€0,20	€0,21	€0,25	€0,16	€0,10	€0,14	€0,25	€0,31	€0,43	€0,56	€0,69
Asset Turnover	*72,8%*	*75,6%*	*72,9%*	*63,3%*	*44,1%*	*38,6%*	*41,6%*	*46,4%*	*50,4%*	*55,9%*	*58,2%*	*59,9%*

APPENDIX 7 – SEGMENT LEVEL REVENUE BUILD

Fiscal Period	FY-19A	FY-20A	FY-21A	FY-22A	FY-23A	FY-24A	FY-25E	FY-26E	FY-27E	FY-28E	FY-29E	FY-30E
Segment Level Revenue Build												
Segment Revenue												
Advanced Logic MEMS	204,4	329,5	391,7	548,9	409,3	480,2	487,0	565,4	655,3	751,3	852,5	938,8
HBM MEMS	–	–	–	–	–	–	–	65,5	96,7	235,7	358,6	557,7
Silicon Photonics Testing	–	–	–	–	–	–	–	–	46,3	72,2	108,0	134,6
Final Testing	–	–	–	–	–	63,0	139,6	145,1	150,9	156,8	163,0	169,5
Aggregate Revenue	**204,4**	**329,5**	**391,7**	**548,9**	**409,3**	**543,2**	**626,6**	**776,0**	**949,2**	**1.216,1**	**1.482,1**	**1.800,5**
Segment EBITDA												
Advanced Logic MEMS	85,8	158,9	174,7	245,4	122,7	130,8	180,7	226,2	262,1	308,0	358,0	394,3
HBM MEMS	–	–	–	–	–	–	–	23,6	40,6	99,0	150,6	234,2
Silicon Photonics	–	–	–	–	–	–	–	–	11,6	24,2	45,4	56,5
Final Testing	–	–	–	–	–	9,5	20,9	24,7	30,2	35,3	40,8	46,6
Aggregate EBITDA	**85,8**	**158,9**	**174,7**	**245,4**	**122,7**	**140,2**	**201,6**	**274,4**	**344,5**	**466,5**	**594,8**	**731,7**
Aggregate EBITDA Margin	*42,0%*	*48,2%*	*44,6%*	*44,7%*	*30,0%*	*25,8%*	*32,2%*	*35,4%*	*36,3%*	*38,4%*	*40,1%*	*40,6%*
Segment Revenue % of Total												
Advanced Logic MEMS	*100,0%*	*100,0%*	*100,0%*	*100,0%*	*100,0%*	*88,4%*	*77,7%*	*72,9%*	*69,0%*	*61,8%*	*57,5%*	*52,1%*
HBM MEMS	*0,0%*	*0,0%*	*0,0%*	*0,0%*	*0,0%*	*0,0%*	*0,0%*	*8,4%*	*10,2%*	*19,4%*	*24,2%*	*31,0%*
Silicon Photonics Testing	*0,0%*	*0,0%*	*0,0%*	*0,0%*	*0,0%*	*0,0%*	*0,0%*	*0,0%*	*4,9%*	*5,9%*	*7,3%*	*7,5%*
Final Testing	*0,0%*	*0,0%*	*0,0%*	*0,0%*	*0,0%*	*11,6%*	*22,3%*	*18,7%*	*15,9%*	*12,9%*	*11,0%*	*9,4%*
Total %	*100,0%*	*100,0%*	*100,0%*	*100,0%*	*100,0%*	*100,0%*	*100,0%*	*100,0%*	*100,0%*	*100,0%*	*100,0%*	*100,0%*
Segment EBITDA % of Total												
Advanced Logic MEMS	*100,0%*	*100,0%*	*100,0%*	*100,0%*	*100,0%*	*93,3%*	*89,6%*	*82,4%*	*76,1%*	*66,0%*	*60,2%*	*53,9%*
HBM MEMS	*0,0%*	*0,0%*	*0,0%*	*0,0%*	*0,0%*	*0,0%*	*0,0%*	*8,6%*	*11,8%*	*21,2%*	*25,3%*	*32,0%*
Silicon Photonics Testing	*0,0%*	*0,0%*	*0,0%*	*0,0%*	*0,0%*	*0,0%*	*0,0%*	*0,0%*	*3,4%*	*5,2%*	*7,6%*	*7,7%*
Final Testing	*0,0%*	*0,0%*	*0,0%*	*0,0%*	*0,0%*	*6,7%*	*10,4%*	*9,0%*	*8,8%*	*7,6%*	*6,9%*	*6,4%*
Total %	*100,0%*	*100,0%*	*100,0%*	*100,0%*	*100,0%*	*100,0%*	*100,0%*	*100,0%*	*100,0%*	*100,0%*	*100,0%*	*100,0%*
Advanced Logic MEMS Segment		236,2	273,0	315,5	364,6	421,3						
(+)TPRO Historic Revenue	204,4	329,5	391,7	548,9	409,3	543,2	626,6					
(-) DIS Revenue	–	–	–	–	–	(63,0)	(139,6)					
Advanced Logic Revenue	**204,4**	**329,5**	**391,7**	**548,9**	**409,3**	**480,2**	**487,0**	565,4	655,3	751,3	852,5	938,8
Advanced Logic Growth		*61,3%*	*18,9%*	*40,1%*	*-25,4%*	*17,3%*	*1,4%*	*16,1%*	*15,9%*	*14,7%*	*13,5%*	*10,1%*
Advanced Logic EBITDA	85,8	158,9	174,7	245,4	122,7	130,8	180,7	226,2	262,1	308,0	358,0	394,3
Advanced Logic EBITDA Margin	*42,0%*	*48,2%*	*44,6%*	*44,7%*	*30,0%*	*27,2%*	*37,1%*	*40,0%*	*40,0%*	*41,0%*	*42,0%*	*42,0%*
Advanced Logic Sub-segment (Revenue)												
Consumer			251,1	341,8	228,2	240,1	225,7	239,2	253,6	268,8	284,9	302,0
Data Center			60,3	82,9	59,5	98,0	105,6	117,9	131,6	146,8	163,9	182,9
Auto/Industrial			80,4	113,9	81,9	73,5	81,6	90,4	100,0	110,7	122,6	135,7
AI GPU			–	10,4	39,7	68,6	57,6	68,0	80,2	94,7	111,7	131,8
ASIC			–	–	–	–	9,6	49,9	89,9	130,3	169,4	186,4
Advanced Logic Sub-segment (%share)												
Consumer			64,1%	62,3%	55,8%	50,0%	47,0%	42,3%	38,7%	35,8%	33,4%	32,2%
Data Center			15,4%	15,1%	14,5%	20,4%	22,0%	20,9%	20,1%	19,5%	19,2%	19,5%
AI GPU			20,5%	20,8%	20,0%	15,3%	17,0%	16,0%	15,3%	14,7%	14,4%	14,5%
Auto/Industrial			–	1,9%	20,0%	14,3%	12,0%	12,0%	12,2%	12,6%	13,1%	14,0%
ASIC			–	–	–	–	2,0%	8,8%	13,7%	17,3%	19,9%	19,9%
Advanced Logic Sub-segment (YoY Growth)												
Consumer			–	36,1%	(33,2%)	5,2%	(6,0%)	*6,0%*	*6,0%*	*6,0%*	*6,0%*	*6,0%*
Data Center			–	37,5%	(28,2%)	64,6%	7,8%	*11,6%*	*11,6%*	*11,6%*	*11,6%*	*11,6%*
Auto/Industrial			–	41,8%	(28,2%)	(10,2%)	11,1%	*10,7%*	*10,7%*	*10,7%*	*10,7%*	*10,7%*
AI GPU			–	–	283,2%	72,8%	(16,0%)	*18,0%*	*18,0%*	*18,0%*	*18,0%*	*18,0%*
ASIC			–	–	–	–	–	*420,0%*	*80,0%*	*45,0%*	*30,0%*	*10,0%*
HBM MEMS Segment												
Total Market Value				2.100,0	3.700,0	17.500,0	34.000,0	42.500,0	53.125,0	66.406,3	83.007,8	103.759,8
Market CAGR				–	76,2%	373,0%	94,3%	*25,0%*	*25,0%*	*25,0%*	*25,0%*	*25,0%*
Test Intensity				*0,7%*	*0,8%*	*0,9%*	*1,0%*	*1,0%*	*1,0%*	*1,0%*	*1,0%*	*1,0%*
HBM Test Market Value				14,7	29,6	157,5	340,0	425,0	531,3	664,1	830,1	1.037,6
SK Hynix Market Share				*50,0%*	*51,3%*	*52,5%*	*62,0%*	*53,0%*	*50,0%*	*49,0%*	*48,0%*	*46,0%*
Samsung Market Share				*40,0%*	*41,2%*	*42,4%*	*17,0%*	*22,0%*	*26,0%*	*31,0%*	*33,0%*	*35,0%*
Micron Market Share				*10,0%*	*7,6%*	*5,1%*	*21,0%*	*25,0%*	*24,0%*	*20,0%*	*19,0%*	*19,0%*
TPRO share of SK Hynix				*0,0%*	*0,0%*	*0,0%*	*0,0%*	*0,0%*	*0,0%*	*20,0%*	*30,0%*	*45,0%*
TPRO share of Samsung				*0,0%*	*0,0%*	*0,0%*	*0,0%*	*70,0%*	*70,0%*	*70,0%*	*70,0%*	*70,0%*
TPRO share of Micron				*0,0%*	*0,0%*	*0,0%*	*0,0%*	*0,0%*	*0,0%*	*20,0%*	*30,0%*	*45,0%*
TPRO Market Share (aggregate)				*0,0%*	*0,0%*	*0,0%*	*0,0%*	*15,4%*	*18,2%*	*35,5%*	*43,2%*	*53,8%*
HBM MEMS Revenue				–	–	–	–	65,5	96,7	235,7	358,6	557,7
HBM MEMS Revenue Growth				*0,0%*	*0,0%*	*0,0%*	*0,0%*	*0,0%*	*47,7%*	*143,8%*	*52,1%*	*55,5%*
HBM MEMS EBITDA				–	–	–	–	23,6	40,6	99,0	150,6	234,2
HBM MEMS EBITDA Margin								*36,0%*	*42,0%*	*42,0%*	*42,0%*	*42,0%*
Final Testing Segment												
Total Device Interface Board Market Value						744,0	773,8	804,7	836,9	870,4	905,2	941,4
Interface Board Market CAGR							*4,0%*	*4,0%*	*4,0%*	*4,0%*	*4,0%*	*4,0%*
Technoprobe Market Share						*8,5%*	*18,0%*	*18,0%*	*18,0%*	*18,0%*	*18,0%*	*18,0%*
DIS Revenue						63,0	139,6	145,1	150,9	156,8	163,0	169,5
Final Testing Revenue Growth						–	*121,6%*	*4,0%*	*4,0%*	*4,0%*	*4,0%*	*4,0%*
Final Testing EBITDA						9,5	20,9	24,7	30,2	35,3	40,8	46,6
Final Testing EBITDA Margin						*15,0%*	*15,0%*	*17,0%*	*20,0%*	*22,5%*	*25,0%*	*27,5%*
Silicon Photonics Segment												
Total Silicon Photonics Chips Market Value					800,0	997,2	1.242,9	1.549,2	1.931,0	2.406,9	3.000,0	3.739,3
Silicon Photonics Chips Market CAGR						*24,6%*	*24,6%*	*24,6%*	*24,6%*	*24,6%*	*24,6%*	*24,6%*
Silicon Photonics Test Market as % of Die Market					*12,0%*	*12,0%*	*12,0%*	*12,0%*	*12,0%*	*12,0%*	*12,0%*	*12,0%*
Total Silicon Photonics Probe Market					96,0	119,7	149,1	185,9	231,7	288,8	360,0	448,7
Technoprobe Market Share					*0,0%*	*0,0%*	*0,0%*	*0,0%*	*20,0%*	*25,0%*	*30,0%*	*30,0%*
Silicon Photonics Revenue					–	–	–	–	46,34	72,21	108,00	134,62
Silicon Photonics Revenue Growth					–	–	–	–	*0,0%*	*55,8%*	*49,6%*	*24,6%*
Silicon Photonics EBITDA					–	–	–	–	11,6	24,2	45,4	56,5
Silicon Photonics EBITDA Margin					–	–	–	–	*25,0%*	*33,5%*	*42,0%*	*42,0%*

APPENDIX 8 – DISCOUNTED CASH FLOW ANALYSIS

In EUR Millions	2020A	2021A	2022A	2023A	2024A	2025E	2026E	2027E	2028E	2029E	2030E
Revenues	**329,5**	**391,7**	**548,9**	**409,3**	**543,2**	**626,6**	**776,0**	**949,2**	**1.216,1**	**1.482,1**	**1.800,5**
% Growth		*18,9%*	*40,1%*	*-25,4%*	*32,7%*	*15,4%*	*23,8%*	*22,3%*	*28,1%*	*21,9%*	*21,5%*
EBITDA	**158,9**	**174,7**	**245,4**	**122,7**	**136,5**	**201,6**	**274,4**	**344,5**	**466,5**	**594,8**	**731,7**
% EBITDA Margin	*48,2%*	*44,6%*	*44,7%*	*30,0%*	*25,1%*	*32,2%*	*35,4%*	*36,3%*	*38,4%*	*40,1%*	*40,6%*
EBIT	**142,4**	**149,9**	**208,4**	**79,8**	**67,1**	**113,4**	**196,9**	**249,7**	**345,1**	**446,8**	**551,9**
% EBIT Margin	*43,2%*	*38,3%*	*38,0%*	*19,5%*	*12,4%*	*18,1%*	*25,4%*	*26,3%*	*28,4%*	*30,1%*	*30,7%*
(-) Taxes	35,2	33,1	59,0	(12,1)	34,2	27,2	47,3	59,9	82,8	107,2	132,5
Tax Rate	*25,7%*	*21,7%*	*28,5%*	*-14,2%*	*35,3%*	*24,0%*	*24,0%*	*24,0%*	*24,0%*	*24,0%*	*24,0%*
NOPAT	**107,2**	**116,8**	**149,4**	**92,0**	**32,9**	**86,2**	**149,7**	**189,8**	**262,3**	**339,6**	**419,4**
% NOPAT Margin	*32,5%*	*29,8%*	*27,2%*	*22,5%*	*6,1%*	*13,8%*	*19,3%*	*20,0%*	*21,6%*	*22,9%*	*23,3%*
+ D&A	16,5	25,0	36,7	43,0	57,3	62,6	77,5	94,8	121,4	148,0	179,8
(-) Capex	(51,3)	(58,9)	(78,4)	(59,1)	(93,5)	(89,8)	(104,5)	(119,5)	(142,6)	(160,9)	(179,8)
% of Revenues	*(15,6%)*	*(15,0%)*	*(14,3%)*	*(14,4%)*	*(17,2%)*	*(14,3%)*	*(13,5%)*	*(12,6%)*	*(11,7%)*	*(10,9%)*	*(10,0%)*
(-) Change in NWC	(41,7)	(44,6)	(9,1)	(23,1)	(12,7)	13,9	(33,7)	(46,7)	(69,3)	(67,6)	(81,4)
% of Revenues	*(12,7%)*	*(11,4%)*	*(1,7%)*	*(5,6%)*	*(2,3%)*	*2,2%*	*(4,3%)*	*(4,9%)*	*(5,7%)*	*(4,6%)*	*(4,5%)*
FCFO	**30,8**	**38,3**	**98,6**	**52,8**	**(15,9)**	**72,9**	**89,0**	**118,3**	**171,8**	**259,1**	**338,0**
Year						0,09	1,09	2,09	3,09	4,09	5,09
Discount Factor						0,992	0,906	0,827	0,755	0,689	0,629
PV of FCFO						**72,3**	**80,6**	**97,9**	**129,7**	**178,5**	**212,7**

In EUR Millions	2031E	2032E	2033E	2034E	2035E	2036E	2037E	2038E	2039E	2040E	2041E
Revenues	**2.160,6**	**2.506,3**	**2.857,2**	**3.200,1**	**3.552,1**	**3.907,3**	**4.298,0**	**4.641,9**	**4.966,8**	**5.264,8**	**5.528,1**
% Growth	*20,0%*	*16,0%*	*14,0%*	*12,0%*	*11,0%*	*10,0%*	*10,0%*	*8,0%*	*7,0%*	*6,0%*	*5,0%*
EBITDA	**889,4**	**1.045,0**	**1.206,4**	**1.280,0**	**1.420,8**	**1.562,9**	**1.719,2**	**1.856,8**	**1.986,7**	**2.105,9**	**2.211,2**
% EBITDA Margin	*41,2%*	*41,7%*	*42,2%*	*40,0%*	*40,0%*	*40,0%*	*40,0%*	*40,0%*	*40,0%*	*40,0%*	*40,0%*
EBIT	**673,7**	**794,8**	**921,2**	**960,5**	**1.066,2**	**1.172,8**	**1.290,1**	**1.393,3**	**1.490,9**	**1.580,3**	**1.659,3**
% EBIT Margin	*31,2%*	*31,7%*	*32,2%*	*30,0%*	*30,0%*	*30,0%*	*30,0%*	*30,0%*	*30,0%*	*30,0%*	*30,0%*
(-) Taxes	161,7	190,7	221,1	230,5	255,9	281,5	309,6	334,4	357,8	379,3	398,2
Tax Rate	*24,0%*	*24,0%*	*24,0%*	*24,0%*	*24,0%*	*24,0%*	*24,0%*	*24,0%*	*24,0%*	*24,0%*	*24,0%*
NOPAT	**512,0**	**604,0**	**700,1**	**730,0**	**810,3**	**891,4**	**980,5**	**1.058,9**	**1.133,0**	**1.201,0**	**1.261,1**
% NOPAT Margin	*23,7%*	*24,1%*	*24,5%*	*22,8%*	*22,8%*	*22,8%*	*22,8%*	*22,8%*	*22,8%*	*22,8%*	*22,8%*
+ D&A	215,7	250,2	285,3	319,5	354,6	390,1	429,1	463,4	495,9	525,6	551,9
(-) Capex	(215,7)	(250,2)	(285,3)	(319,5)	(354,6)	(390,1)	(429,1)	(463,4)	(495,9)	(525,6)	(551,9)
% of Revenues	*(10,0%)*	*(10,0%)*	*(10,0%)*	*(10,0%)*	*(10,0%)*	*(10,0%)*	*(10,0%)*	*(10,0%)*	*(10,0%)*	*(10,0%)*	*(10,0%)*
(-) Change in NWC	(75,5)	(87,6)	(99,9)	(111,9)	(124,2)	(136,6)	(150,2)	(162,3)	(173,6)	(184,0)	(193,2)
% of Revenues	*(3,5%)*	*(3,5%)*	*(3,5%)*	*(3,5%)*	*(3,5%)*	*(3,5%)*	*(3,5%)*	*(3,5%)*	*(3,5%)*	*(3,5%)*	*(3,5%)*
FCFO	**436,5**	**516,4**	**600,2**	**618,2**	**686,2**	**754,8**	**830,2**	**896,7**	**959,4**	**1.017,0**	**1.067,8**
Year	6,09	7,09	8,09	9,09	10,09	11,09	12,09	13,09	14,09	15,09	16,09
Discount Factor	0,574	0,524	0,479	0,437	0,399	0,364	0,332	0,304	0,277	0,253	0,231
PV of FCFO	**250,7**	**270,8**	**287,3**	**270,1**	**273,7**	**274,9**	**276,0**	**272,2**	**265,9**	**257,3**	**246,6**

Tgt. EBITDA Margin	*40,0%*
Tax Rate	*24,0%*
Capex % of Revenues	*(10,0%)*
NWC % of Revenue	*(3,5%)*
WACC	*9,5%*
LT Growth Rate (g)	*2,0%*

PV of FCFO	3.717,2
% of EV	*52,7%*
Terminal Value	14.448,0
PV of TV	3.336,7
% of EV	*47,3%*
Enterprise Value	**7.053,9**
(-) Net Debt	656,83
EqV	**7.710,7**
Diluted ShO	651,76
Price/Share	€ 11,83
Current Price	€ 15,63
Upside/Downside	*-24,3%*

APPENDIX 9 – TPRO VS. FORM MULTIPLES ANALYSIS

All Comps	EV/Sales (x)				EV/EBITDA (x)				P/E (x)			
	Actual	FY+1	FY+2	FY+3	Actual	FY+1	FY+2	FY+3	Actual	FY+1	FY+2	FY+3
TPRO Metric	543.2	626.9	747.3	899.7	136.4	201.7	268.0	354.7	0.1	0.2	0.3	0.3
Multiple Avg.	11.3x	8.8x	7.2x	6.5x	43.0x	35.9x	30.0x	24.9x	60.7x	57.9x	43.8x	34.3x
Implied EV/EqV	6151.8	5513.5	5365.5	5803.3	5870.0	7238.8	8031.7	8835.8	6.1	9.3	11.0	11.7
Net Debt	656.83											
Implied EqV	6808.6	6170.3	6022.3	6460.2	6526.8	7895.6	8688.6	9492.6				
Diluted ShO	651.76											
Price per Share	10.4	9.5	9.2	9.9	10.0	12.1	13.3	14.6	6.1	9.3	11.0	11.7
Market Price	15.63											
Upside/Downside	*-33.2%*	*-39.4%*	*-40.9%*	*-36.6%*	*-35.9%*	*-22.5%*	*-14.7%*	*-6.8%*	*-61.1%*	*-40.8%*	*-29.9%*	*-25.3%*

vs. FORM	EV/Sales (x)				EV/EBITDA (x)				P/E (x)			
	Actual	FY+1	FY+2	FY+3	Actual	FY+1	FY+2	FY+3	Actual	FY+1	FY+2	FY+3
TPRO Metric	543.2	626.9	747.3	899.7	136.4	201.7	268.0	354.7	0.1	0.2	0.3	0.3
FORM Multiple	6.9x	7.5x	6.8x	6.5x	43.0x	43.0x	33.7x	26.6x	60.8x	66.9x	48.9x	41.7x
Implied EV/EqV	3733.1	4715.6	5088.2	5803.3	5870.0	8680.2	9036.1	9438.0	6.1	10.7	12.2	14.2
Net Debt	656.83											
Implied EqV	4390.0	5372.5	5745.0	6460.2	6526.8	9337.0	9693.0	10094.8				
Diluted ShO	651.76											
Price per Share	6.7	8.2	8.8	9.9	10.0	14.3	14.9	15.5	6.1	10.7	12.2	14.2
Market Price	15.63											
Upside/Downside	*-56.9%*	*-47.3%*	*-43.6%*	*-36.6%*	*-35.9%*	*-8.3%*	*-4.8%*	*-0.9%*	*-61.1%*	*-31.5%*	*-21.7%*	*-9.3%*

APPENDIX 10 – COMPARABLE COMPANIES ANALYSIS

	EV/Sales (x)				EV/EBITDA (x)				P/E (x)			
Company	Actual	FY+1	FY+2	FY+3	Actual	FY+1	FY+2	FY+3	Actual	FY+1	FY+2	FY+3
Technoprobe	17.5x	15.1x	12.7x	10.5x	69.5x	47.0x	35.4x	26.7x	155.5x	97.2x	62.2x	45.7x
FormFactor	6.9x	7.5x	6.8x	6.5x	43.0x	43.0x	33.7x	26.6x	60.8x	66.9x	48.9x	41.7x
Advantest	18.7x	17.1x	14.1x	12.0x	57.2x	39.4x	30.0x	24.9x	92.2x	57.9x	44.1x	35.0x
Teradyne	11.4x	11.6x	9.5x	8.1x	46.0x	46.1x	33.5x	26.7x	63.7x	65.4x	43.8x	33.9x
TSMC	11.3x	8.8x	7.2x	6.0x	16.4x	12.4x	10.1x	8.9x	26.3x	20.1x	16.7x	14.0x
Intel	4.0x	4.9x	4.8x	4.5x	21.5x	19.5x	15.5x	12.2x	N/A	139.7x	77.9x	44.5x
ASML	15.6x	13.6x	12.7x	11.0x	44.5x	35.9x	33.4x	26.9x	60.6x	47.0x	43.2x	34.3x
SK Hynix	7.1x	5.6x	3.2x	2.8x	13.0x	9.1x	4.6x	4.0x	24.5x	13.4x	6.8x	6.1x
Median	10.7x	9.9x	8.3x	7.3x	34.5x	29.3x	23.0x	18.6x	54.7x	58.6x	40.2x	29.9x
Average	11.3x	8.8x	7.2x	6.5x	43.0x	35.9x	30.0x	24.9x	60.7x	57.9x	43.8x	34.3x

	EBITDA Margin				CapEx/Revenue				Cash Conversion Cycle				
Company	Actual	FY+1	FY+2	FY+3	Actual	FY+1	FY+2	FY+3	DIO	DPO	DSO	CCC	Operating Cycle
Technoprobe	*25.1%*	*32.2%*	*35.9%*	*39.4%*	*17.3%*	*10.4%*	*15.0%*	*11.5%*	135.47	46.83	97.57	186.20	233.04
FormFactor	*16.0%*	*17.5%*	*20.2%*	*24.2%*	*5.0%*	*13.8%*	*13.2%*	*4.2%*	83.76	42.88	62.87	103.75	146.63
Advantest	*32.7%*	*43.3%*	*47.2%*	*48.1%*	*2.5%*	*3.4%*	*2.6%*	*2.1%*	203.75	103.66	51.87	151.96	255.62
Teradyne	*24.7%*	*25.2%*	*28.2%*	*30.2%*	*7.0%*	*6.7%*	*5.0%*	*4.7%*	232.14	57.79	68.85	243.20	300.99
TSMC	*68.9%*	*70.9%*	*70.8%*	*67.8%*	*33.4%*	*31.3%*	*28.8%*	*24.9%*	69.16	18.75	28.04	78.45	97.20
Intel	*18.7%*	*25.2%*	*30.8%*	*37.3%*	*41.8%*	*33.0%*	*30.4%*	*29.2%*	124.86	115.07	21.91	31.70	146.77
ASML	*35.2%*	*37.9%*	*38.0%*	*40.8%*	*7.4%*	*5.6%*	*54.6%*	*5.1%*	277.68	N/A	75.69	N/A	353.37
SK Hynix	*54.5%*	*61.4%*	*70.7%*	*69.6%*	*24.1%*	*27.0%*	*20.7%*	*19.1%*	126.05	19.88	58.57	164.73	184.62
Median	*35.8%*	*40.2%*	*43.7%*	*45.5%*	*17.3%*	*17.3%*	*22.2%*	*12.8%*	159.63	59.67	52.54	128.97	212.17
Average	*32.7%*	*37.9%*	*38.0%*	*40.8%*	*7.4%*	*13.8%*	*20.7%*	*5.1%*	126.05	50.34	58.57	127.85	184.62

	EV/CapEx (x)				P/CapEx (x)				EBITDA Margin			
Company	Actual	FY+1	FY+2	FY+3	Actual	FY+1	FY+2	FY+3	Actual	FY+1	FY+2	FY+3
Technoprobe	100.9x	144.8x	84.7x	92.0x	107.8x	154.7x	90.6x	98.3x	*25.1%*	*32.2%*	*35.9%*	*39.4%*
FormFactor	136.4x	54.5x	51.7x	152.4x	143.8x	57.5x	54.5x	160.7x	*16.0%*	*17.5%*	*20.2%*	*24.2%*
Advantest	755.3x	502.1x	544.7x	568.8x	765.2x	508.7x	551.9x	576.3x	*32.7%*	*43.3%*	*47.2%*	*48.1%*
Teradyne	161.6x	173.5x	187.2x	172.5x	164.8x	176.9x	191.0x	175.9x	*24.7%*	*25.2%*	*28.2%*	*30.2%*
TSMC	33.9x	28.1x	24.9x	24.2x	35.5x	29.4x	26.1x	25.3x	*68.9%*	*70.9%*	*70.8%*	*67.8%*
Intel	9.6x	14.8x	15.7x	15.5x	9.0x	13.8x	14.6x	14.5x	*18.7%*	*25.2%*	*30.8%*	*37.3%*
ASML	212.2x	243.6x	23.3x	217.0x	214.4x	246.2x	23.5x	219.3x	*35.2%*	*37.9%*	*38.0%*	*40.8%*
SK Hynix	29.4x	20.7x	15.6x	14.6x	29.9x	21.0x	15.8x	14.9x	*54.5%*	*61.4%*	*70.7%*	*69.6%*
Median	191.2x	148.2x	123.3x	166.4x	194.7x	150.5x	125.4x	169.6x	*35.8%*	*40.2%*	*43.7%*	*45.5%*
Average	136.4x	54.5x	24.9x	152.4x	143.8x	57.5x	26.1x	160.7x	*32.7%*	*37.9%*	*38.0%*	*40.8%*